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Revision 0.6
Preliminary - Confidential

LMX9820A
Bluetooth™ Serial Port Module

1.0 General Description

The National Semiconductor® LMX9820A Bluetooth™ Serial Port module is a highly integrated radio, baseband controller and memory device implemented on an FR4 substrate. All hardware and firmware is included to provide a complete solution from antenna through the complete lower and upper layers of the Bluetooth stack, up to the application including the Generic Access Profile (GAP), the Service Discovery Application Profile (SDAP), and the Serial Port Profile (SPP). The module includes a configurable service database to fulfil service requests for additional profiles on the host. The LMX9820A features a small form factor (10.1 x 14.0 x 1.9 mm) design; thus, solving many of the challenges associated with system integration. Moreover, the LMX9820A is pre-qualified as a Bluetooth Integrated Component. Conformance testing through the Bluetooth qualification program enables a short time to market after system integration by insuring a high probability of compliance and interoperability.

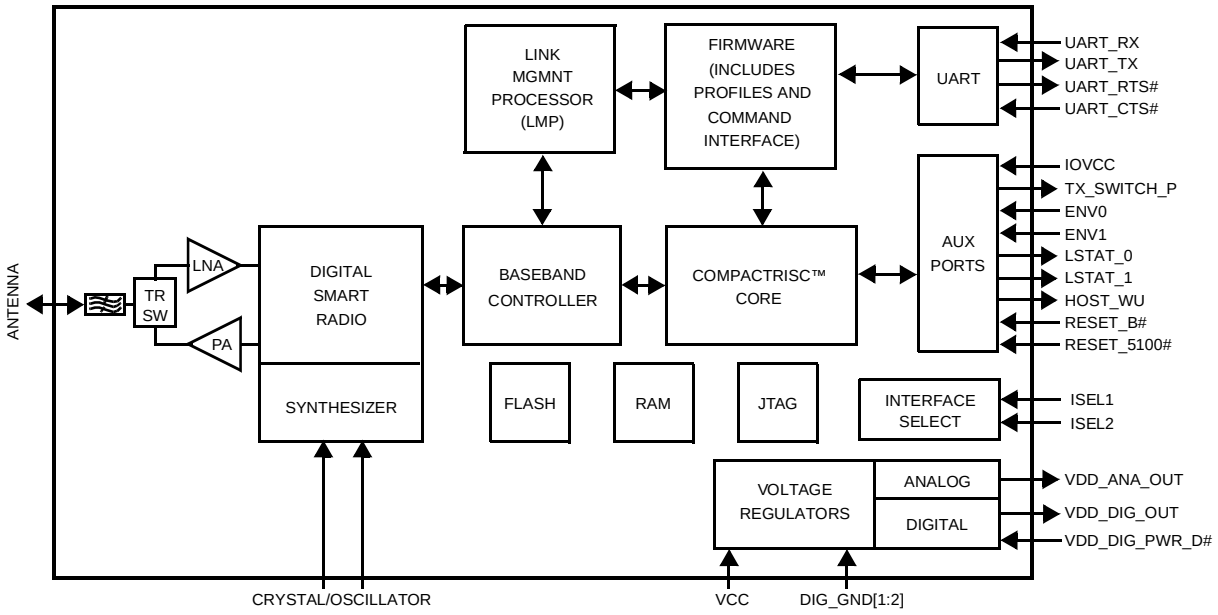
Based on National's CompactRISC™ 16-bit processor architecture and Digital Smart Radio technology, the LMX9820A is optimized to handle the data and link management processing requirements of a Bluetooth node.

The firmware supplied within this device offers a complete Bluetooth (v1.1) stack including profiles and command interface. This firmware features point-to-point and point-to-multipoint link management supporting data rates up to the theoretical maximum over RFComm of 704 kbps. The internal memory supports up to three active Bluetooth links.

1.1 APPLICATIONS

- Personal Digital Assistants
- POS Terminals
- Data Logging Systems

2.0 Functional Block Diagram



3.0 Features

- Bluetooth version 1.1 qualified
- Implemented in CMOS technology on FR4 substrate.
- Temperature Range: -40°C to +85°C

3.1 DIGITAL HARDWARE

- Baseband and Link Management processors
- CompactRISC Core
- Integrated Memory:
  - Flash
  - RAM
- UART Command/Data Port:
  - Support for up to 921.6k baud rate
- Auxiliary Host Interface Ports:
  - Link Status
  - Transceiver Status (Tx or Rx)
  - Operating Environment Control:
    - Default Bluetooth mode
    - In System Programming (ISP) mode
- Advanced Power Management (APM) features

3.2 FIRMWARE

- Complete Bluetooth Stack including:
  - Baseband and Link Manager
  - L2CAP, RFCOMM, SDP
  - Profiles:
    - GAP
    - SDAP
    - SPP
- Additional Profile support on Host for:
  - Dial Up Networking (DUN)
  - Facsimile Profile (FAX)
  - File Transfer Protocol (FTP)
  - Object Push Profile (OPP)
  - Synchronization Profile (SYNC)
- On-chip application including:
  - Command Interface:
    - Link setup and configuration (also Multipoint)
    - Configuration of the module
    - In system programming
    - Service database modifications
    - Default connections
  - UART Transparent mode
  - Different Operation modes:
    - Automatic mode
    - Command mode

3.3 DIGITAL SMART RADIO

- Accepts external clock or crystal input:
  - 12 MHz
  - 20 ppm cumulative clock error required for Bluetooth
- Synthesizer:
  - Integrated VCO and loop filter
  - Provides all clocking for radio and baseband functions
- Antenna Port (50 Ohms nominal impedance):
  - Embedded front-end filter for enhanced out of band performance
- Integrated transmit/receive switch (full duplex operation via antenna port)
- Better than -77 dBm input sensitivity
- 0 dBm typical output power

3.4 PHYSICAL

- Compact size - 10.1mm x 14.0mm x 1.9mm
- Complete system interface provided in Land Grid Array on underside for surface mount assembly
- Metal shield included

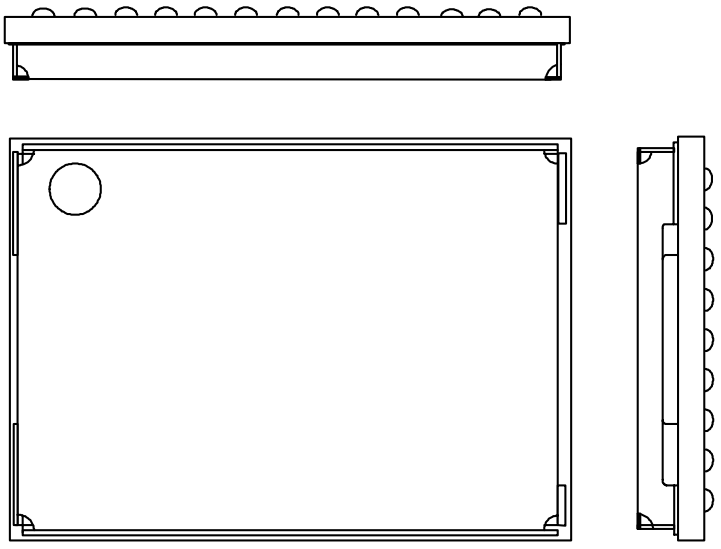


Figure 1. Physical Illustration

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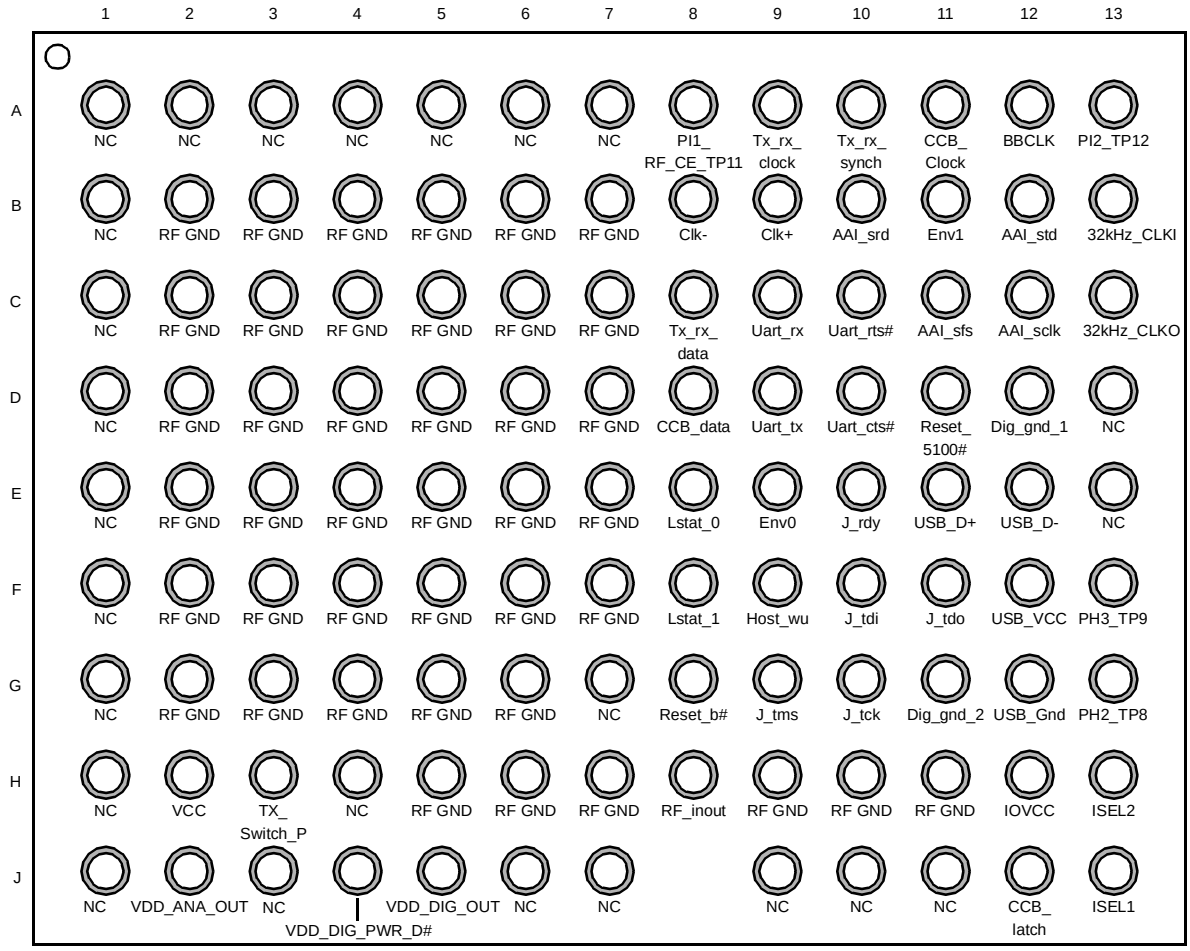
4.0 Connection Diagram



X-Ray (Top View)

Figure 2. Connection Diagram LMX9820A

Table 1. Order Information

Order Number	Shipment Method
LMX9820ASM	Tape & Reel 250pcs
LMX9820ASMX	Tape & Reel 2000pcs

5.0 Pad Descriptions

Table 2. System Interface Signals

Pad Name	Pad Location	Direction	Description
Clk-	B8	Input	**Xtal g or Negative Clock Input.** Typically connected along with XTAL_D to an external surface mount AT cut crystal. Can also be configured as a frequency input when using an external crystal oscillator. When configured as a frequency input, typically connected to Ground with a 10 pF capacitor.
Clk+	B9	Input	**Xtal d or Positive Clock Input.** Typically connected along with XTAL_G to an external surface mount AT cut crystal. Can also be configured as a frequency input when using an external crystal oscillator. When configured as a frequency input, is typically connected to an external Temperature Compensated Crystal Oscillator (TCXO) through an Alternating Current (AC) coupling capacitor.
32kHz_CLKI	B13	Input	**32 kHz Clock input.** Used for low power modes.
32kHz_CLKO	C13	Output	**32 kHz Clock Output.** Used for low power modes.
RF_inout	H8	Input/Output	**RF Antenna Port.** 50Ω nominal impedance. Typically connected to an antenna through a 6.8pF capacitor.
ISEL2	H13	Input	**Module Interface Select Input Bit 1.**
ISEL1	J13	Input	**Module Interface Select Input Bit 0.**

Table 3. USB Interface Signals (Not supported by LMX9820A firmware)

Pad Name	Pad Location	Direction	Description
USB_VCC	F12	Input	**USB Transceiver Power Supply +** [1]
USB_D+	E11	Input/Output	**USB Data Positive** [1]
USB_D-	E12	Input/Output	**USB Data Negative** [1]
USB_Gnd	G12	Input	**USB Transceiver Ground** [1]

1. Treat as No Connect, Pad required for mechanical stability.

Table 4. UART Interface Signals

Pad Name	Pad Location	Direction	Description
Uart_tx	D9	Output	**UART Host Control Interface Transport, Transmit Data.**
Uart_rx	C9	Input	**UART Host Control Interface Transport, Receive Data.**
Uart_rts#	C10	Output	**UART Host Control Interface Transport, Request to Send.**
Uart_cts#	D10	Input	**UART Host Control Interface Transport, Clear to Send.**

Table 5. Auxiliary Ports Interface Signals

Pad Name	Pad Location	Direction	Description
IOVCC	H12	Input	**2.85V to 3.6V Logic Threshold Program Input.**
Reset_b#	G8	Input	**Reset Input for Smart Radio.** Normally connected to Reset_5100.

5.0 Pad Descriptions (Continued)

Table 5. Auxiliary Ports Interface Signals (Continued)

Pad Name	Pad Location	Direction	Description
Reset_5100#	D11	Input	**Reset for Baseband and Link Management Processors.** Active low.
Lstat_0	E8	Output	**Link Status Bit 0.**
Lstat_1	F8	Output	**Link Status Bit 1.**
Host_wu	F9	Output	**Host Wakeup**
Env0	E9	Input	**Module Operating Environment Bit 0.**
Env1	B11	Input	**Module Operating Environment Bit 1.**
TX_Switch_P	H3	Output	**Transceiver Status,** 0 = Receive; 1 = Transmit.

Table 6. Audio Port Interface Signals

Pad Name	Pad Location	Direction	Description
AAI_srd	B10	Input	**Advanced Audio Interface Receive Data Input.**[1]
AAI_std	B12	Output	**Advanced Audio Interface Transmit Data Output.**[1]
AAI_sfs	C11	Input/Output	**Advanced Audio Interface Frame Synchronization.**[1]
AAI_sclk	C12	Input/Output	**Advanced Audio Interface Clock.**[1]

1. Treat as No Connect if not used, Pad required for mechanical stability.

Table 7. Test Interface Signals

Pad Name	Pad Location	Direction	Description
J_rdy	E10	Output	**JTAG Ready.**[1]
J_tdi	F10	Input	**JTAG Test Data.**[1]
J_tdo	F11	Input/Output	**JTAG Test Data.**[1]
J_tms	G9	Input/Output	**JTAG Test Mode Select.**[1]
J_tck	G10	Input	**JTAG Test Clock.** [1]
PI1_RFCE_TP11	A8	Testpin	**Module Test Point.**[1]
PI2_TP12	A13	Testpin	**Module Test Point.**[1]
Tx_rx_clock	A9	Testpin	**Module Test Point.**[1]
Tx_rx_data	C8	Testpin	**Module Test Point.**[1]
Tx_rx_synch	A10	Testpin	**Module Test Point.**[1]
CCB_Clock	A11	Testpin	**Module Test Point.**[1]
CCB_data	D8	Testpin	**Module Test Point.**[1]
CCB_latch	J12	Testpin	**Module Test Point.**[1]
BBCLK	A12	Testpin	**Module Test Point.**[1]
PH3_TP9	F13	Testpin	**Module Test Point.**[1]
PH2_TP8	G13	Testpin	**Module Test Point.**[1]

5.0 Pad Descriptions (Continued)

1. Treat as No Connect, Pad required for mechanical stability.

Table 8. Power, Ground, and No Connect Signals

Pad Name	Pad Location	Direction	Description
NC	A1, A2, A3, A4, A5, A6, A7, B1, C1, D1, D13, E1, E13, F1, G1, G7, H1, H4, J1, J3, J6, J7, J9, J10, J11	not connected	**No Connect.** Must have pad for mechanical stability.
RF GND[1]	B2, B3, B4, B5, B6, B7, C2, C3, C4, C5, C6, C7, D2, D3, D4, D5, D6, D7, E2, E3, E4, E5, E6, E7, F2, F3, F4, F5, F6, F7, G2, G3, G4, G5, G6, H5, H6, H7, H9, H10, H11	Input	**Radio System Ground.** Must be connected to RF Ground plane. Thermal relief required for proper soldering.
Dig_gnd_1[1]	D12	Input	**Digital Ground.**
Dig_gnd_2[1]	G11	Input	**Digital Ground.**
VCC	H2	Input	**2.85V to 3.6V Input for the Internal Power Supply Regulators.**
VDD_ANA_OUT	J2	Output	**Voltage Regulator Output/Power Supply for Analog Circuitry.** If not used, place pad and do not connect to VCC or Ground.
VDD_DIG_OUT	J5	Output	**Voltage Regulator Output/Power Supply for Digital Circuitry.** If not used, place pad and do not connect to VCC or Ground.
VDD_DIG_PWR_D#	J4	Input	**Power Down for the Internal Power Supply Regulator for the Digital Circuitry.** Place pad and do not connect to VCC or Ground.

1. Connect RF GND, Dig_gnd_1, and Dig_gnd_2 to single Ground plane.

6.0 Electrical Specifications

6.1 GENERAL SPECIFICATIONS

Absolute Maximum Ratings (see Table 9) indicate limits beyond which damage to the device may occur. Operating Ratings (see Table 10) indicate conditions for which the device is intended to be functional.

This device is a high performance RF integrated circuit and is ESD sensitive. Handling and assembly of this device should be performed at ESD free workstations.

The following conditions are true unless otherwise stated in the tables below:

- T_A = -40°C to +85°C
- VCC = 3.3V
- RF system performance specifications are guaranteed on National Semiconductor Austin Board rev1.0b reference design platform.

Table 9. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VCC	Core Logic Power Supply Voltage	-0.3	3.6	V
IOVCC	I/O Power Supply Voltage	-0.3	3.6	V
USB_VCC[1]	USB Power Supply Voltage	-0.5	3.63	V
V_I	Voltage on any pad with GND = 0V	-0.5	VCC + 0.5	V
PinRF	RF Input Power		+15	dBm
T_S	Storage Temperature Range	-65	+150	^oC
T_L	Lead Temperature (solder 4 sec)		+260	^oC
ESD-HBM	ESD - Human Body Model		2000	V
ESD-MM	ESD - Machine Model		200[2]	V

1. USB Interface not supported by LMX9820A firmware. Treat as no connect, place pad for mechanical stability.
2. Maximum ESD-MM for antenna pin is 150V.

Table 10. Recommended Operating Conditions[1]

Symbol	Parameter	Min	Typ[2]	Max	Unit
VCC	Module Power Supply Voltage	2.85	3.3	6	V
IOVCC	I/O Power Supply Voltage	2.85	3.3	6	V
USB_VCC[3]	USB Power Supply Voltage	2.97	3.3	3.63	V
t_R	Module Power Supply Rise Time			50	ms
T_O	Operating Temperature Range	-40		+85	°C
HUM_{OP}	Humidity (operating, across operating temperature range)	10		90	%
HUM_{NONOP}	Humidity (non-operating, 38.7^{o}C web bulb temperature)	5		95	%

1. Maximum voltage difference allowed between VCC and IOVCC is 500 mV.
2. Typical operating conditions are at 3.3V operating voltage and 25°C ambient temperature.
3. USB Interface not supported by LMX9820A firmware. Treat as no connect, place pad for mechanical stability.

Table 11. Power Supply Electrical Specifications: Analog and Digital LDOs

Symbol	Parameter	Min	Typ[1]	Max	Unit
VDD_ANA_OUT	Analog Voltage Output Range		2.8		V
VDD_DIG_OUT	Digital Voltage Output Range		2.5		V

1. Typical operating conditions are at 3.3V operating voltage and 25^{o}C ambient temperature.

6.0 Electrical Specifications (Continued)

NOTE: The voltage regulators are optimized for the internal operation of the LMX9820A. As any noise or coupling into those can have influence on the radio performance, it is highly recommended to have no additional load on those outputs.

Table 12. Power Supply Requirements[1,2,3]

Symbol	Parameter	Min	Typ	Max	Unit
I_{CC-TX}	Power supply current for continous transmit		48	60	mA
I_{CC-RX}	Power supply current for continous receive		43	50	mA
I_{RXSL}	Receive Data in SPP Link, Slave[4]		15		mA
I_{RXM}	Receive Data in SPP Link, Master[4]		18		mA
I_{SnM}	Sniff Mode, Sniffintervall 1 second[4]		8		mA
$I_{SC-TLDIS}$	Scanning, No Active Link, TL Disabled[4]		3		mA
I_{Idle}	Idle, Scanning Disabled, TL Disabled[4]		0.25		mA

1. Power supply requirements based on Class II output power.
2. VCC = 3.0V, IOVCC = 3.3V, Ambient Temperature = +25 °C.
3. Based on UART Baudrate 115.2kbit/s.
4. Average values

6.2 DC CHARACTERISTICS

Table 13. Digital DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
VCC	Core Logic Supply Voltage		2.85	3.6	V
IOVCC	IO Supply Voltage		2.85	3.6	V
V_{IH}	Logical 1 Input Voltage		0.7*IOVCC	IOVCC + 0.5	V
V_{IL}	Logical 0 Input Voltage		-0.5	0.2*IOVCC	V
V_{XL2}[1]	32.768kHz Logical 0 Input Voltage	External 32.768kHz clock	-0.5	0.3*IOVCC	V
V_{XH2}[1]	32.768kHz Logical 1 Input Voltage	External 32.768kHz clock	0.7*IOVCC	IOVCC + 0.5	V
V_{HYS}	Hysteresis Loop Width[2]		0.1*IOVCC		V
I_{OH}	Logical 1 Output Current	V_{OH} = 1.8V, IOVCC = 2.25V	-1.6		mA
I_{OL}	Logical 0 Output Current	V_{OL} = 0.45V, IOVCC = 2.25V	1.6		mA
I_{OHW}	Weak Pull-up Current	V_{OH} = 1.8V, IOVCC = 2.25V	-10		µA
I_{IH}	High-level Input Current	V_{IH} = IOVCC = 2.85V	- 1.0	1.0	µA
I_{IL}[3]	Low-level Input Current	V_{IL} = 0	- 1.0	1.0	µA
I_L	High Impedance Input Leakage Current	$0V \le V_{IN} \le IOVCC$	-2.0	2.0	µA
$I_{O(Off)}$	Output Leakage Current (I/O pins in input mode)	$0V \le V_{OUT} \le VCC$	-2.0	2.0	µA

1. Not supported, please place pad and leave unconnected.
2. Guaranteed by design.
3. Limit for I_{IL} for the pins Reset_b#, PI1_RFCE_TP & VDD_DIG_PWR_D# is +/-3uA.

6.0 Electrical Specifications (Continued)

6.3 RF PERFORMANCE CHARACTERISTICS

In the performance characteristics tables the following applies:

- All tests performed are based on Bluetooth Test Specification rev 0.91.
- All tests are measured at antenna port unless otherwise specified
- T_A = -40°C to +85°C
- VCC = 3.3V unless otherwise specified

RF system performance specifications are guaranteed on National Semiconductor Austin Board rev1.0b reference design platform.

Table 14. Receiver Performance Characteristics

Symbol	Parameter	Condition		Min	Typ[1]	Max	Unit
RX_{sense} [2]	Receive Sensitivity	BER < 0.001	2.402 GHz		-84	-74	dBm
			2.441 GHz		-84	-74	dBm
			2.480 GHz		-84	-74	dBm
PinRF	Maximum Input Level			-10	0		dBm
C/I_{CCI} [3]	Carrier to Interferer Ratio in the Presence of Co-channel Interferer	$P_{in}RF$ = -60 dBm, BER < 0.001			10		dB
C/I_{ACI} [4]	Carrier to Interferer Ratio in the Presence of Adjacent Channel Interferer	$\Delta F_{ACI} = \pm 1$ MHz, $P_{in}RF$ = -60 dBm, BER < 0.001			-1		dB
		$\Delta F_{ACI} = \pm 2$ MHz. $P_{in}RF$ = -60 dBm, BER < 0.001			-37		dB
		ΔF_{ACI} = + 3 MHz, $P_{in}RF$ = -67 dBm, BER < 0.001			-47		dB
C/I_{IMAGE} - 1MHz	Carrier to Interferer Ratio in the Presence of Image-1MHz Interferer	Δf = -3 MHz, PinRF = -67 dBm, BER < 0.001			-32		dB
IMP[5]	Intermodulation Performance	F_1= + 3 MHz, F_2= + 6 MHz, $P_{in}RF$ = -64 dBm		-38	-36		dBm
RSSI	RSSI Dynamic Range at LNA Input			-72		-52	dBm
Z_{RFIN}	Input Impedance of RF Port (RF_inout)	Single input impedance F_{in} = 2.5 GHz			50		Ω
Return Loss	Return Loss					-8	dB
OOB	Out Of Band Blocking Performance	$P_{in}RF$ = -10 dBm, 30 MHz < F_{CWI} < 2 GHz, BER < 0.001		-10			dBm
		$P_{in}RF$ = -27 dBm, 2000 MHz < F_{CWI} < 2399 MHz, BER < 0.001		-27			dBm
		$P_{in}RF$ = -27 dBm, 2498 MHz < F_{CWI} < 3000 MHz, BER < 0.001		-27			dBm
		$P_{in}RF$ = -10 dBm, 3000 MHz < F_{CWI} < 12.75 GHz, BER < 0.001		-10			dBm

6.0 Electrical Specifications (Continued)

1.Typical operating conditions are at 2.85V operating voltage and 25°C ambient temperature.
2.The receiver sensitivity is measured at the device interface.
3. Not tested in production.
4. Not tested in production.
5.The f_0 = -64 dBm Bluetooth modulated signal, f_1 = -39dbm sine wave, f_2 = -39 dBm Bluetooth modulated signal, $f_0 = 2f_1 - f_2$, and $|f_2 - f_1| = n * 1MHz$, where n is 3, 4, or 5. For the typical case, n = 3.

Table 15. Transmitter Performance Characteristics

Symbol	Parameter	Condition	Min	Typ[1]	Max	Unit
$P_{OUT}RF$[2]	Transmit Output Power	2.402 GHz	-2	+1	+3	dBm
		2.441 GHz	-2	+1	+3	dBm
		2.480 GHz	-2	+1	+3	dBm
Power Density	Power Density		-4	1	2	dBm
MOD $\Delta F1_{AVG}$	Modulation Characteristics	Data = 00001111	140	165	175	kHz
MOD $\Delta F2_{MAX}$[3]	Modulation Characteristics	Data = 10101010	115	125		kHz
$\Delta F2_{AVG}/\Delta F1_{AVG}$[4]	Modulation Characteristics		0.8			
20 dB Bandwidth					1000	kHz
ACP[5]	Adjacent Channel Power (In-band Spurious)	| M - N | = 2		-48	-20	dBm
		| M - N | ≥ 3		-51	-40	dBm
$P_{OUT}2*f_o$[6]	PA 2nd Harmonic Suppression	Maximum gain setting: f_0 = 2402 MHz, P_{out} = 4804 MHz			-35	dBm
$P_{OUT}3*f_o$[3]	PA 3rd Harmonic Suppression	Maximum gain setting: f_0 = 2402 MHz, P_{out} = 7206 MHz			-32	dBm
Z_{RFOUT}	RF Output Impedance/Input Impedance of RF Port (RF_inout)	P_{out} @ 2.5 GHz		50		Ω
Return Loss	Return Loss				-14	dB

1.Typical operating conditions are at 2.85V operating voltage and 25°C ambient temperature.
2.The output power is measure at the device interface.
3.$\Delta F2max \geq 115$ kHz for at least 99.9% of all $\Delta f2max$.
4.Modulation index set between 0.28 and 0.35.
5.Not tested in production.
6.Out-of-Band spurs only exist at 2nd and 3rd harmonics of the CW frequency for each channel.

Table 16. Synthesizer Performance Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{VCO}	VCO Frequency Range			5000		MHz
t_{LOCK}	Lock Time	$f_0 \pm 20$ kHz		120		µs
Δf_0offset[1]	Initial Carrier Frequency Tolerance	During preamble	-75	0	75	kHz

6.0 Electrical Specifications (Continued)

Table 16. Synthesizer Performance Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$\Delta f_0 drift^2$	Initial Carrier Frequency Drift	DH1 data packet	-25	0	25	kHz
		DH3 data packet	-40	0	40	kHz
		DH5 data packet	-40	0	40	kHz
		Drift Rate	-20	0	20	kHz/50µs
t_D-Tx	Transmitter Delay Time	From Tx data to antenna		4		µs

1. Frequency accuracy is dependent on crystal oscillator chosen. The crystal must have a cumulative accuracy of < +/-20ppm to meet Bluetooth specifications.
2. Frequency accuracy is dependent on crystal oscillator chosen. The crystal must have a cumulative accuracy of < +/-20ppm to meet Bluetooth specifications.

6.4 PERFORMANCE DATA (TYPICAL)

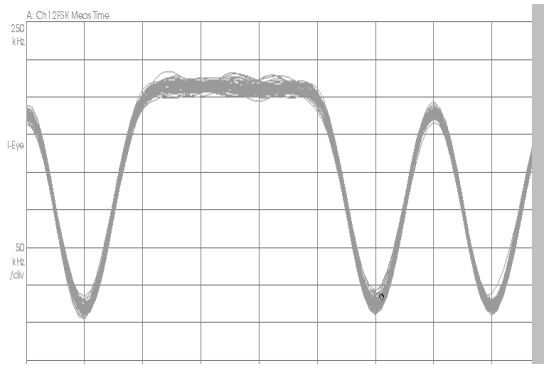


Figure 3. Modulation

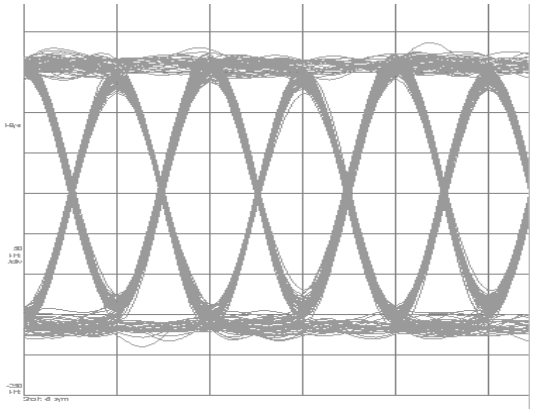


Figure 5. Corresponding Eye Diagram

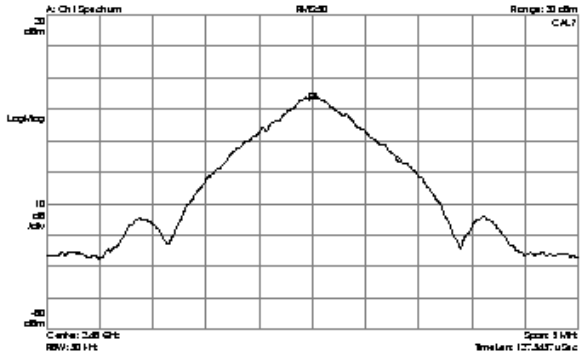


Figure 4. Transmit Spectrum

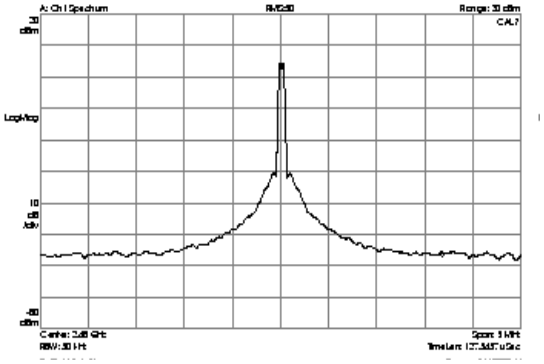


Figure 6. Synthesizer Phase Noise

6.0 Electrical Specifications (Continued)

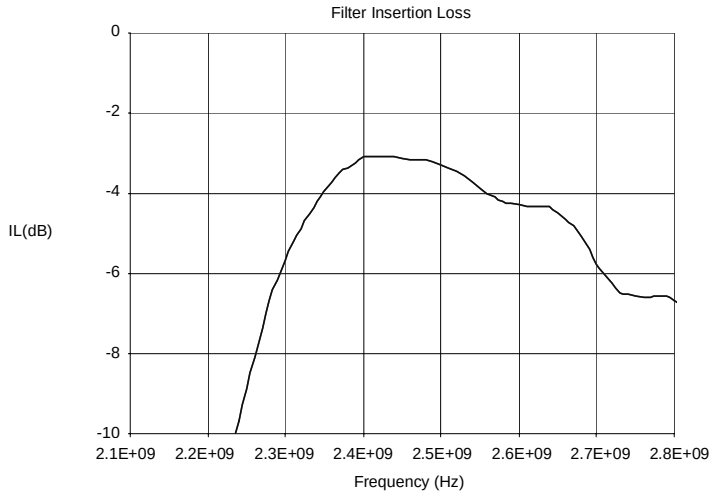


Figure 7. Front-End Bandpass Filter Response

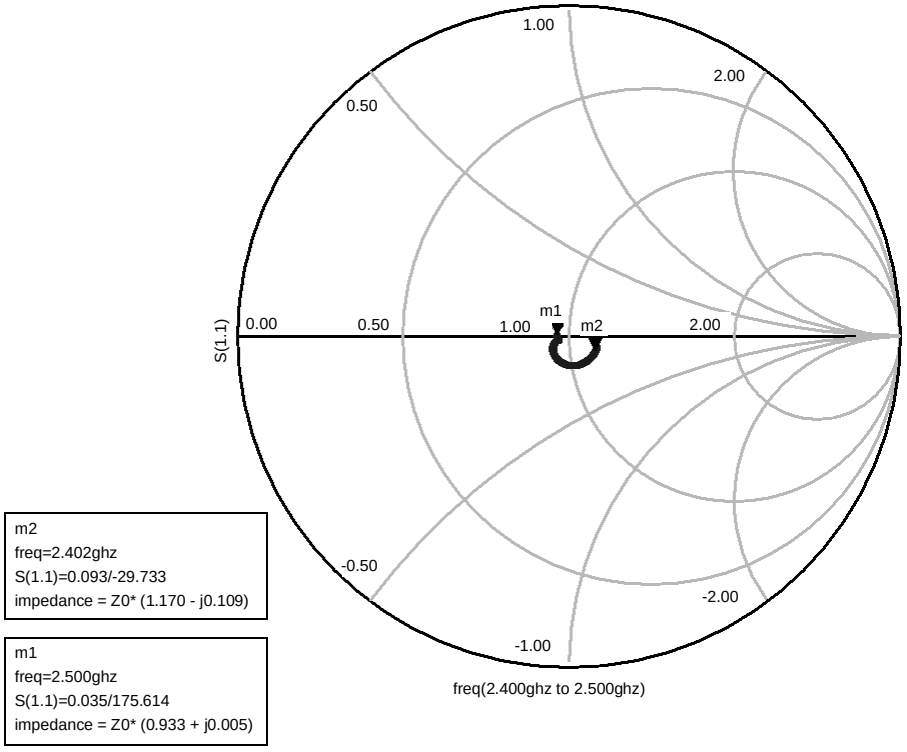


Figure 8. TX and RX Pin 50Ω Impedance Characteristics

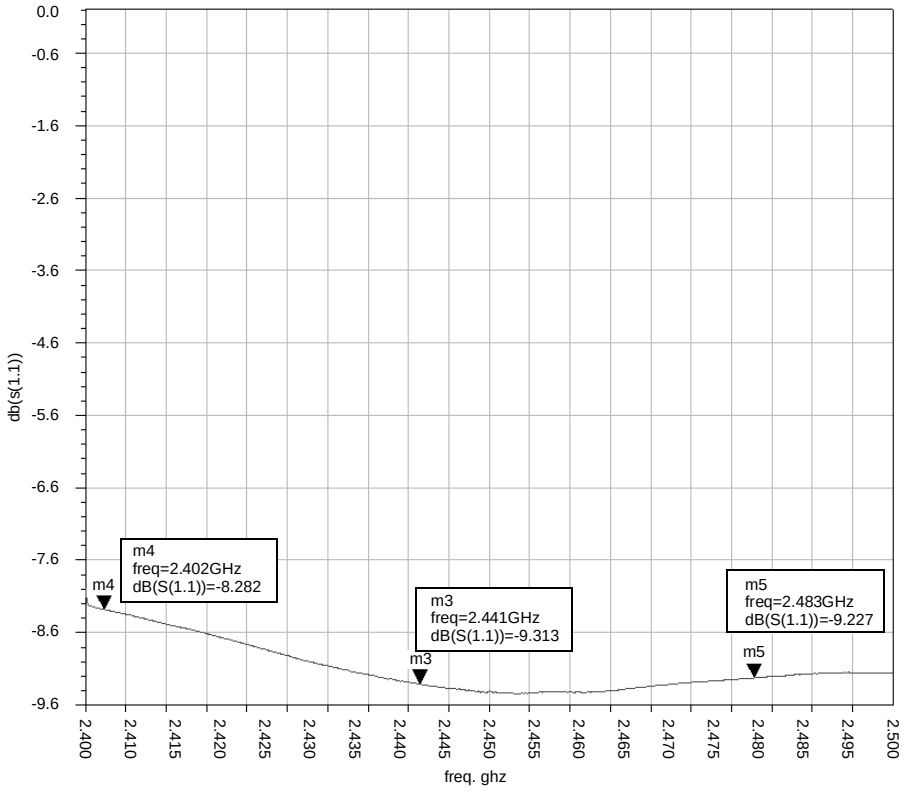


Figure 9. Transceiver Return Loss

7.0 Functional Description

7.1 BASEBAND AND LINK MANAGEMENT PROCESSORS

Baseband and Lower Link control functions are implemented using a combination of National Semiconductor's CompactRISC 16-bit processor and the Bluetooth Lower Link Controller. These processors operate from integrated Flash memory and RAM and execute on-board firmware implementing all Bluetooth functions.

7.1.1 Bluetooth Lower Link Controller

The integrated Bluetooth Lower Link Controller (LLC) complies with the Bluetooth Specification version 1.1 and implements the following functions:

- Support for 1, 3, and 5 slot packet types
- 79 Channel hop frequency generation circuitry
- Fast frequency hopping at 1600 hops per second
- Power management control
- Access code correlation and slot timing recovery

7.1.2 Bluetooth Upper Layer Stack

The integrated upper layer stack is prequalified and includes the following protocol layers:

- L2CAP
- RFComm
- SDP

7.1.3 Profile support

The on-chip application of the LMX9820A allows full standalone operation, without any Bluetooth protocol layer necessary outside the module. It supports the Generic Access Profile (GAP), the Service Discovery Application Profile (SDAP), and the Serial Port Profile (SPP).

The on-chip profiles can be used as interfaces to additional profiles executed on the host. The LMX9820A includes a configurable service database to answer requests with the profiles supported.

7.1.4 Application with command interface

The module supports automatic slave operation eliminating the need for an external control unit. The implemented transparent option enables the chip to handle incoming data raw, without the need for packaging in a special format. The device uses a fixed pin to block unallowed connections.

Acting as master, the application offers a simple but versatile command interface for standard Bluetooth operation like inquiry, service discovery, or serial port connection. The firmware supports up to three slaves. Default Link Policy settings and a specific master mode allow optimized configuration for the application specific requirements. See also Section "Integrated Firmware" on page 24.

7.2 MEMORY

The LMX9820A includes 256kB of programmable Flash memory that can be used for code and constant data. It allows single cycle read access from the CPU. In addition

to storing all algorithms and firmware, the on-board Flash also contains the IEEE 802 compliant Media Access Controller (MAC) address (BDADDR). The firmware and the BDADDR are programmed by National Semiconductor or can be programmed by the customer either before assembly into the host system or in system. Module firmware can be updated as well during manufacturing or by the consumer using the ISP capabilities of the LMX9820A. The LMX9820A firmware uses the internal RAM for buffers and program variables.

7.3 CONTROL AND TRANSPORT PORT

The LMX9820A provides one Universal Asynchronous Receiver Transmitter (UART). It supports 8-bit data formats with or without parity and one or two stop bits. The baud rate is generated by hardware that is programmed at boot time. Alternatively, the speed and configuration settings can be read out of internal memory settings. The UART can operate at baud rates of 2.4k, 4.8k, 7.2k, 9.6k, 19.2k, 38.4k, 57.6k, 115.2k, 230.4k, 460.8k and 921.6k. It implements flow control logic (RTS, CTS) to provide hardware handshaking capability. The UART offers wakeup from the power save modes via the multi-input wakeup module. UART logic thresholds are set via the IOVCC pin.

7.4 AUXILIARY PORTS

7.4.1 Reset_5100 and Reset_b

Reset_5100 and Reset_b are active low reset inputs for the baseband controller and digital smart radio portions of the LMX9820A, respectively. These pins are normally tied together and are connected to the host system so that the host can initialize the LMX9820A by asserting the reset inputs. Upon removal, the status of the module operating environment (Env) pads are sampled and the LMX9820A enters the corresponding operational mode.

7.4.2 Operating Environment Pads (Env0 and Env1)

The module provides two operating environments (see Table 17) depending on the state of the Env pads after the removal of the reset inputs. At power up of the module, Env0 and Env1 are checked to determine which operating environment straps are selected and operating.

The ISP mode allows end-of-line or field programming of the LMX9820A Flash memory by starting the baseband controller from the boot block of memory.

Table 17. Operating Environments

Operating Environment	Env1 (Pad B11)	Env0 (Pad E9)
ISP Mode	1	0
Run (Normal) Mode (Default)	1	1

7.4.3 Interface Select Inputs (ISEL1, ISEL2)

The interface selection pads are used for setting the UART speed and settings. As ISEL1 and ISEL2 are set by internal weak-pull-ups, the default baudrate is 921.6kbit/s. The settings for Stopbits, Startbit and Parity are stored as internal NVS parameter. If a baudrate different to the listed needs to be used, ISEL 1 and ISEL2 have to be set to 0. This forces the device to get also the UART speed from the parameter table. The default baudrate value set in NVS is 9.6kbit/s. Default configuration in NVS is 1 Stopbit, 1 Startbit and No parity.

Table 18 provides the ISEL1 and ISEL2 selection settings.

Table 18. UART Speed Selection

ISEL1 (Pad J13)	ISEL2 (Pad H13)	Interface Speed (baud)	UART Settings
1	1	921.6k	Check NVS
0	1	115.2k	Check NVS
1	0	9.6k	1Stop, 1Start, No Parity
0	0	Check NVS	Check NVS

7.4.4 Module and LInk Status Outputs

The LMX9820A provides signals that the host can use to determine the real-time status of the radio link. The TX_Switch_P signal (pad H3) is a real-time indication of the current configuration (direction) of the transceiver. The link status lines (Lstat_0 and Lstat_1, pads E8 and F8, respectively) are GPIO lines controlled by the LMX9820A firmware. The Host Wakeup line (Host_wu, pad F9) is implemented using GPIO and firmware. It is used to bring the host processor out of Sleep mode when link activity calls for host processing. Host_wu can also be used by the host to check if link activity is present. If Host_wu is active, then link activity is present and the host loses network awareness if the operating system continues to allow the host processor to enter the Sleep mode. Table 19 presents the definitions of the various module and link status outputs.

Table 19. Module / Link Status Definitions

Lstat_0 (Pad E8)	Lstat_1 (Pad F8)	TX_Switch_P (Pad H3)	Host_wu (Pad F9)	Mode
x	1	x	x	At least 1 SPP link established
x	0	x	x	No active SPP link
x	x	1	x	Transceiver = Transmit
x	x	0	x	Transceiver = Receive
x	x	x	0	Host can Sleep
x	x	x	1	Wakeup host/host shouldn't Sleep

8.0 Digital Smart Radio

8.1 FUNCTIONAL DESCRIPTION

The integrated Digital Smart Radio utilizes a heterodyne receiver architecture with a low intermediate frequency (2 MHz) such that the intermediate frequency filters can be integrated on chip. The receiver consists of a low-noise amplifier (LNA) followed by two mixers. The intermediate frequency signal processing blocks consist of a poly-phase bandpass filter (BPF), two hard-limiters (LIM), a frequency discriminator (DET), and a post-detection filter (PDF). The received signal level is detected by a received signal strength indicator (RSSI).

The received frequency equals the local oscillator frequency (fLO) plus the intermediate frequency (fIF):

fRF = fLO + fIF (supradyne).

The radio includes a synthesizer consisting of a phase detector, a charge pump, an (off-chip) loop-filter, an RF-frequency divider, and a voltage controlled oscillator (VCO).

The transmitter utilizes IQ-modulation with bit-stream data that is gaussian filtered. Other blocks included in the transmitter are a VCO buffer and a power amplifier (PA).

8.2 RECEIVER FRONT-END

The receiver front-end consists of a low-noise amplifier (LNA) followed by two mixers and two low-pass filters for the I- and Q-channels.

The intermediate frequency (IF) part of the receiver front-end consists of two IF amplifiers that receive input signals from the mixers, delivering balanced I- and Q-signals to the poly-phase bandpass filter. The poly-phase bandpass filter is directly followed by two hard-limiters that together generate an AD-converted RSSI signal.

8.2.1 Poly-Phase Bandpass Filter

The purpose of the IF bandpass filter is to reject noise and spurious (mainly adjacent channel) interference that would otherwise enter the hard limiting stage. In addition, it takes care of the image rejection.

The bandpass filter uses both the I- and Q-signals from the mixers. The out-of-band suppression should be higher than 40 dB (f<1 MHz, f>3 MHz). The bandpass filter is tuned over process spread and temperature variations by the autotuner circuitry. A 5th order Butterworth filter is used.

8.2.2 Hard-Limiter and RSSI

The I- and Q-outputs of the bandpass filter are each followed by a hard-limiter. The hard-limiter has its own reference current. The RSSI (Received Signal Strength Indicator) measures the level of the RF input signal.

The RSSI is generated by piece-wise linear approximation of the level of the RF signal. The RSSI has a mV/dB scale, and an analog-to-digital converter for processing by the baseband circuit. The input RF power is converted to a 5-bit value. The RSSI value is then proportional to the input power (in dBm).

The digital output from the ADC is sampled on the BPKTCTL signal low-to-high transition.

8.3 RECEIVER BACK-END

The hard-limiters are followed by a two frequency discriminators. The I-frequency discriminator uses the 90× phase-shifted signal from the Q-path, while the Q-discriminator uses the 90× phase-shifted signal from the I-path. A poly-phase bandpass filter performs the required phase shifting. The output signals of the I- and Q-discriminator are substracted and filtered by a low-pass filter. An equalizer is added to improve the eye-pattern for 101010 patterns.

After equalization, a dynamic AFC (automatic frequency offset compensation) circuit and slicer extract the RX_DATA from the analog data pattern. It is expected that the Eb/No of the demodulator is approximately 17 dB.

8.3.1 Frequency Discriminator

The frequency discriminator gets its input signals from the limiter. A defined signal level (independent of the power supply voltage) is needed to obtain the input signal. Both inputs of the frequency discriminator have limiting circuits to optimize performance. The bandpass filter in the frequency discriminator is tuned by the autotuning circuitry.

8.3.2 Post-Detection Filter and Equalizer

The output signals of the FM discriminator first go through a post-detection filter and then through an equalizer. Both the post-detection filter and equalizer are tuned to the proper frequency by the autotuning circuitry. The post-detection filter is a low-pass filter intended to suppress all remaining spurious signals, such as the second harmonic (4 MHz) from the FM detector and noise generated after the limiter.

The post-detection filter also helps for attenuating the first adjacent channel signal. The equalizer improves the eye-opening for 101010 patterns. The post-detection filter is a third order Butterworth filter.

8.4 AUTOTUNING CIRCUITRY

The autotuning circuitry is used for tuning the bandpass filter, the detector, the post-detection filter, the equalizer, and the transmit filters for process and temperature variations. The circuit also includes an offset compensation for the FM detector.

8.5 SYNTHESIZER

The synthesizer consists of a phase-frequency detector, a charge pump, a low-pass loop filter, a programmable frequency divider, a voltage-controlled oscillator (VCO), a delta-sigma modulator, and a lookup table.

The frequency divider consists of a divide-by-2 circuit (divides the 5 GHz signal from the VCO down to 2.5 GHz), a divide-by-8-or-9 divider, and a digital modulus control. The delta-sigma modulator controls the division ratio and also generates an input channel value to the lookup table.

8.5.1 Phase-Frequency Detector

The phase-frequency detector is a 5-state phase-detector. It responds only to transitions, hence phase-error is independent of input waveform duty cycle or amplitude variations. Loop lockup occurs when all the negative transitions on the inputs, F_REF and F_MOD, coincide. Both outputs (i.e., Up and Down) then remain high. This is equal to the

zero error mode. The phase-frequency detector input frequency range operates at 12MHz.

8.6 TRANSMITTER CIRCUITRY

The transmitter consists of ROM tables, two Digital to Analog (DA) converters, two low-pass filters, IQ mixers, and a power amplifier (PA).

The ROM tables generate a digital IQ signal based on the transmit data. The output of the ROM tables is inserted into IQ-DA converters and filtered through two low-pass filters. The two signal components are mixed up to 2.5 GHz by the TX mixers and added together before being inserted into the transmit PA.

8.6.1 IQ-DA Converters and TX Mixers

The ROM output signals drive an I- and a Q-DA converter. Two Butterworth low-pass filters filter the DA output signals. The 6 MHz clock for the DA converters and the logic circuitry around the ROM tables are derived from the autotuner.

The TX mixers mix the balanced I- and Q-signals up to 2.4-2.5 GHz. The output signals of the I- and Q-mixers are summed.

8.7 LOW FREQUENCY CIRCUITRY

The low frequency circuitry includes an adjustable crystal oscillator (XO), an adjustable low power oscillator (LPO), a power-on reset (POR) block, and an off-chip reset input. For generation of the system clock, a 12 MHz crystal or external reference clock input can be used.

For operation in low power modes, the LMX9820A includes 32.768kHz low frequency oscillator circuit. The source can be either a reference clock or crystal signal input. Alternatively, the main system clock can be used.

8.8 EXTERNAL CRYSTAL OSCILLATORS

The LMX9820A contains a crystal driver circuit. This circuit operates with an external crystal and capacitors to form an oscillator. See Figure 10 on page 18 and Figure 11 on page 18. The LMX9820A also can operate with an external TCXO (Temperature Compensated Crystal Oscillator).

8.9 CRYSTAL CIRCUIT TUNING SCOPE

The LMX9820A has a new crystal circuit with a different internal load capacitance than the LMX9820. This requires possible crystal tuning. Included in this section are the details and crystals that have been tested with the LMX9820A. This is for reference and it is highly recommended that each design is carefully reviewed and tested for overall system performance in the process of converting from LMX9820 to the LMX9820A.

The RF local oscillator and internal digital clocks for the LMX9820A Serial Port module is derived from the reference clock at the CLK+ input. This reference may either come from an external clock or a dedicated crystal oscillator. The crystal oscillator connections require an Xtal and two grounded capacitors.

It is also important to consider board and design dependant capacitance in tuning crystal circuit. Equations that follow allow a close approximation of crystal tuning capacitance required, but actual values on board will vary with capacitive properties of the board. As a result, there is some fine tuning of crystal circuit that has to be done that can not be calculated, must be tuned by testing different values of load capacitance.

Many different crystals can be used with the LMX9820A. Key requirements from Bluetooth specification is $\pm$ 20ppm. Additionally, ESR (Equivalent Series Resistance) must be carefully considered. LMX9820A can support maximum of 230ohm ESR, but it is recommended to stay <100ohms ESR for best performance over voltage and temperature. Reference Figure 14 on page 22 for ESR as part of crystal circuit and Section 9.0 for more information.

8.10 XTAL MODE

The LMX9820A crystal driver circuit operates with an external crystal and capacitors to form an oscillator. (See Figure 10 on page 18 and Figure 22 on page 35). The LMX9820A also can also operate with an external TCXO (Temperature Compensated Crystal Oscillator).

8.11 CRYSTAL

The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors. The resonant frequency may be trimmed with the crystal load capacitance.

1. Load Capacitance

For resonance at the correct frequency, the crystal should be loaded with its specified load capacitance, which is the value of capacitance used in conjunction with the crystal unit. Load capacitance is a parameter specified by the crystal, typically expressed in pF. The crystal circuit shown in Figure 11 is composed of:

- C1 (motional capacitance)
- R1 (motional resistance)
- L1 (motional inductance)
- C0 (static or shunt capacitance)

The LMX9820A provide some of the load with internal capacitors C_{int}. The remainder must come from the external capacitors labeled Ct1 and Ct2 as shown in Figure 10. Ct1 and Ct2 should have the same the value for best noise performance. Crystal load capacitance ($C_{L)}$ is calculated as the following:

$C_L = C_{int} + Ct1//Ct2$

The C_L above does not include the crystal internal self-capacitance C0 as shown in Figure 11 on page 18, so the total capacitance is:

$C_{total} = C_L + C0$

8.0 Digital Smart Radio (Continued)

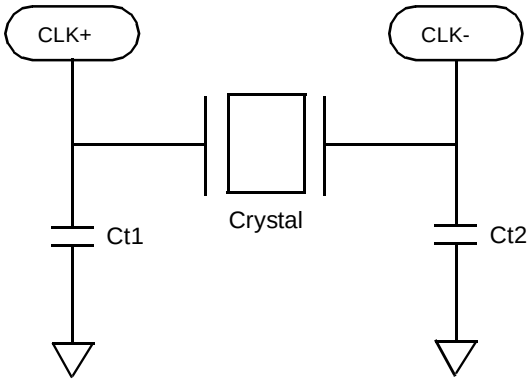


Figure 10. LMX9820A Crystal Recommended Circuit

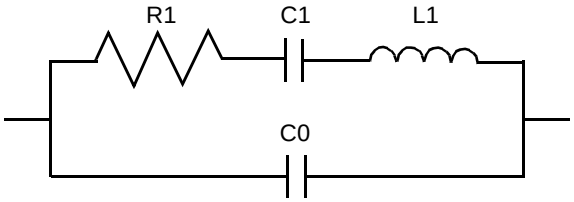


Figure 11. Crystal Equivalent Circuit

2. Crystal Pullability

Pullability is another important parameter for a crystal, which is the change in frequency of a crystal with units of ppm/pF, either from the natural resonant frequency to a load resonant frequency, or from one load resonant frequency to another. The frequency can be pulled in a parallel resonant circuit by changing the value of load capacitance. A decrease in load capacitance causes an increase in frequency, and an increase in load capacitance causes a decrease in frequency.

3. Frequency Tuning

Frequency Tuning is achieved by adjusting the crystal load capacitance with external capacitors. It is a Bluetooth requirement that the frequency is always within ±20 ppm. Crystal/oscillator must have cumulative accuracy specifications of **±15 ppm** to provide margin for frequency drift with ageing and temperature.

8.11.1 Vite Crystal

The VXE4-1055 is a 12 MHz SMT crystal from Vite. National is using this crystal with the LMX9820A. Table 20 on page 18 shows the specification of VXE4-1055.

Since the internal capacitance of the crystal circuit is 4-5 pF and the load capacitance is 9 pF, 10 pF is a good starting point for both Ct1 and Ct2. The 2480 MHz RF frequency offset is then tested. Figure 12 on page 19 shows the RF frequency offset test results.

Figure 12 shows the results are 100 kHz off the center frequency, which is –4 ppm. The pullability of the crystal is 24 ppm/pF, so the load capacitance must be decreased by about 0.2 pF. By changing Ct1 or Ct2 to 9 pF, the total load capacitance is increased by 0.26 pF. Figure 12 on page 19 shows the frequency offset test resuts. The frequency offset is now zero with Ct1 = 9 pF, Ct2 = 10 pF.

Reference Table 21 on page 18 for crystal tuning values used on Austin Development Board with Vite crystal.

Table 20. VXE4-1055-12M000

Specification	Value
Package	6.0x3.5x1.1 mm - 4 pads
Frequency	12.000 MHz
Mode	Fundamental
Stability	±18 ppm at -20 to +70°C (inclusive of all conditions)
Load Capacitance	9 pF
ESR	40 Ω max, 20 Ω typ
Shunt Capacitance	7 pF max
Drive Level	10 to 100 µW
Pullability	24 ppm/pF min
Storage Temperature	-40 to +85°C

Table 21. VXE4-1055-12M000 on Austin Board

Reference	LMX9820	LMX9820A
Ct1	10pF	Not Recommended
Ct2	10pF	Not Recommended

8.11.2 Kinseki KSS CX-4025S

The LMX9820A has also been tested with the Kineski KSS CX-4025S. See Table 22 on page 18.

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Table 22. KSS CX-4025S

Specification	Value
Package	4.0x2.5x0.75 mm - 4 pads
Frequency	12.000 MHz
Mode	Fundamental
Stability	±20 ppm at -30 to +80°C (inclusive of all conditions)
Load Capacitance	12pF
ESR	80 Ω max, 20 Ω typ
Shunt Capacitance	3 pF max
Drive Level	100 µW max
Storage Temperature	-40 to +85°C

Reference Table 4 on page 2 for crystal tuning values used on Austin Development Board with KSS crystal.

8.0 Digital Smart Radio (Continued)

Table 23. KSS CX-4025S on Austin Board

Reference	LMX9820	LMX9820A
Ct1	30pF	6pF
Ct2	30pF	6pF

8.11.3 TEW

The LMX9820A has also been tested with the TEW crystal. See Table 24 on page 19.

Table 24. TEW

Specification	Value
Package	4.0x2.5x0.65 mm - 4 pads
Frequency	12.000 MHz
Mode	Fundamental
Stability	> ±15ppm @-40 to +85C
Load Capacitance	16pF
ESR	80 Ω max.
Shunt Capacitance	5pF
Drive Level	50 ±10uV
Storage Temperature	-40 to +85C

Reference Table 25 on page 19 for crystal tuning values used on Austin Development Board with TEW crystal.

Table 25. TEW on Austin Board

Reference	LMX9820	LMX9820A
Ct1	56pF	10pF
Ct2	56pF	10pF

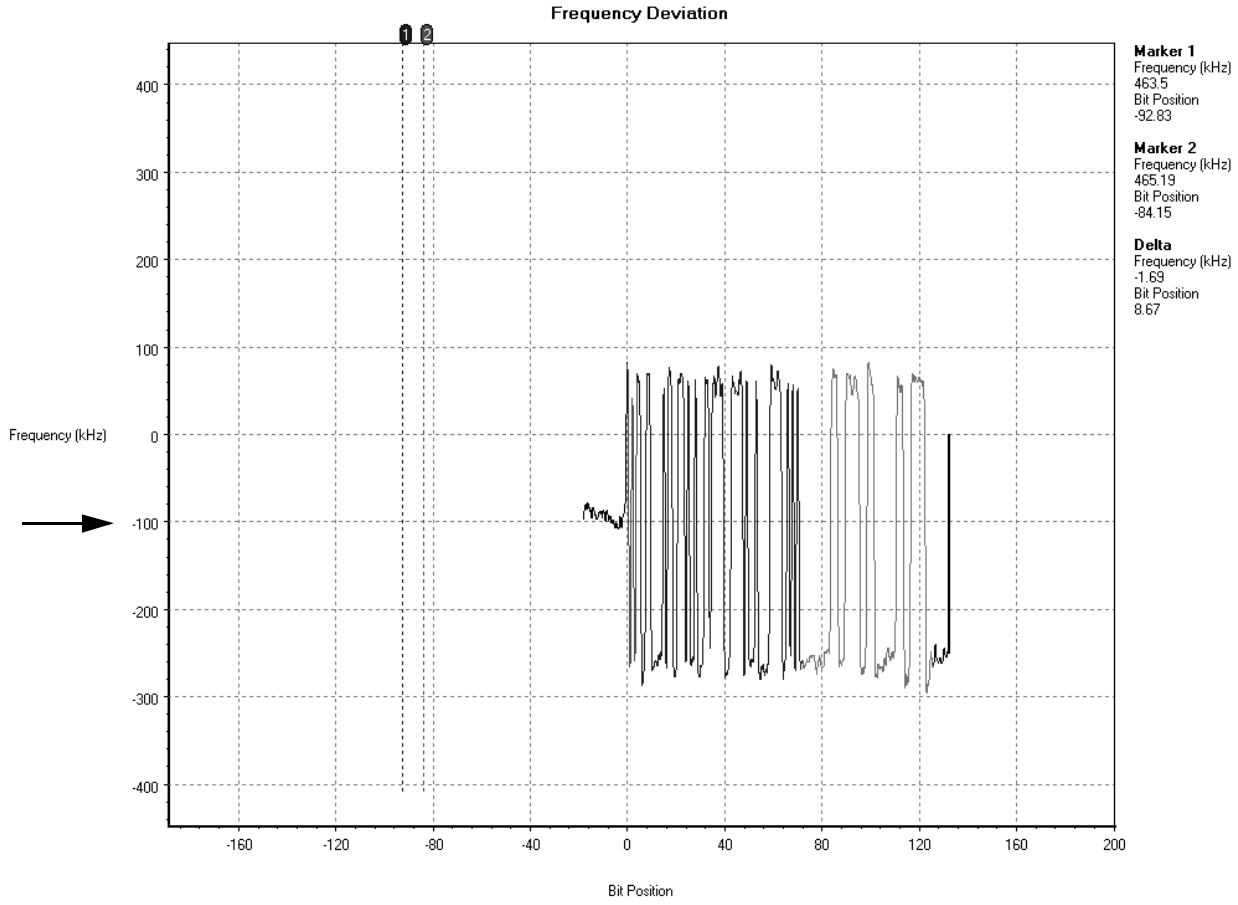

Figure 12. Frequency Offset with 10 pF Capacitors

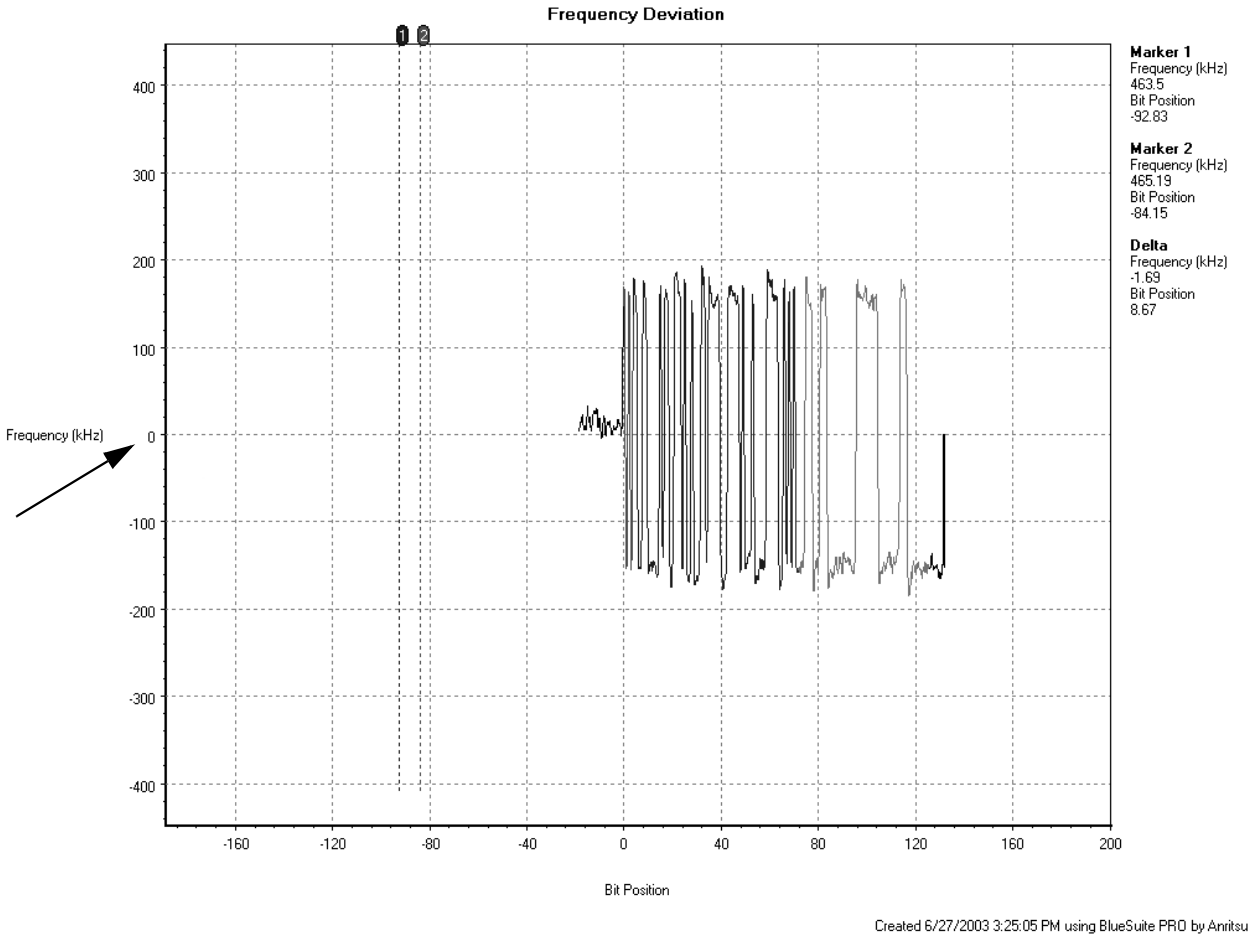

Figure 0-1. Frequency Offset with 9 pF//10 pF Capacitors

8.12 TCXO (TEMPERATURE COMPENSATED CRYSTAL OSCILLATOR)

The LMX9820A also can operate with an external TCXO (Temperature Compensated Crystal Oscillator). The TCXO signal is directly connected to the CLK+, shown in Table 26 on page 20.

1. Input Impedance

The LMX9820A CLK+ pin has in input impedance of 2pF capacitance in parallel with >400kΩ resistance.

2. NKG3184A TCXO

The LMX9820A has also been tested with the NKG3184A TCXO. See Table 26 on page 20.

Table 26. TCXO - NKG3184A

Specification	Value
Package	5.0x3.2x1.4 mm - 4 pads
Frequency	12.000 MHz
Stability	±18 ppm at -30 to +85°C (inclusive of all conditions)
Output Load	10kΩ // 13pF
Current Consumption	2.0mA
Output Level	0.3Vp-p to 2.0Vp-p
Storage Temperature	-40 to +85°C
DC Cut Capacitor	Included in VC-TCXO

8.13 OPTIONAL 32 KHZ OSCILLATOR

A second oscillator is provided (see Figure 13) that is tuned to provide optimum performance and low-power consumption while operating with a 32.768 kHz crystal. An external crystal clock network is required between the 32kHz_CLKI clock input (pad B13) and the 32kHz_CLKO clock output (pad C13) signals.The oscillator is built in a Colpitt configuration and uses two external capacitors. Table 27 provides the oscillator's specifications.

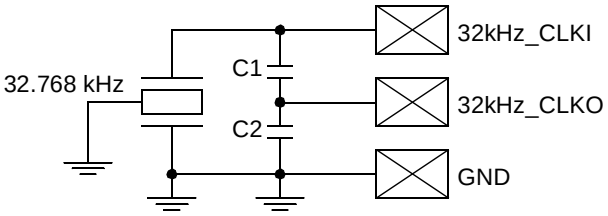

Figure 13. 32.768 kHz Oscillator

Table 27. 32.768 kHz Oscillator Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		2.25	2.5	2.75	V
I_{DDACT}	Supply Current (Active)	Q_{MAX} = 50,000		10		µA
I_{DDPWD}	Supply Current (Power Down)	Q_{MAX} = 50,000			0.1	µA
f	Nominal Output Frequency			32.768		kHz
Δf/f	Total Frequency Error	T_A = -10°C to +70°C		-220 to +150	+/-250	ppm
t_S	Start-up Time	Q_{MAX} = 50,000		5		S
V_{PPOSC}	Oscillating Amplitude			1.8		V
	Duty Cycle		38	48.3	58	%

9.0 ESR (Equivalent Series Resistance)

LMX9820A can operate with a wide range of crystals with different ESR ratings. Reference Table 28 on page 21 and Figure 14 on page 22 for more details.

Table 28. System Clock Requirements

Parameter	Min	Typ	Max	Unit
External Reference Clock Frequency		12MHz		MHz
Frequency Tolerance (over full operating temperature and aging)		±15	±20	ppm
Crystal Serial Resistance			230	Ω
External Reference Clock Power Swing, pk to pk	100	200	400	mV
Aging			±1	ppm per year

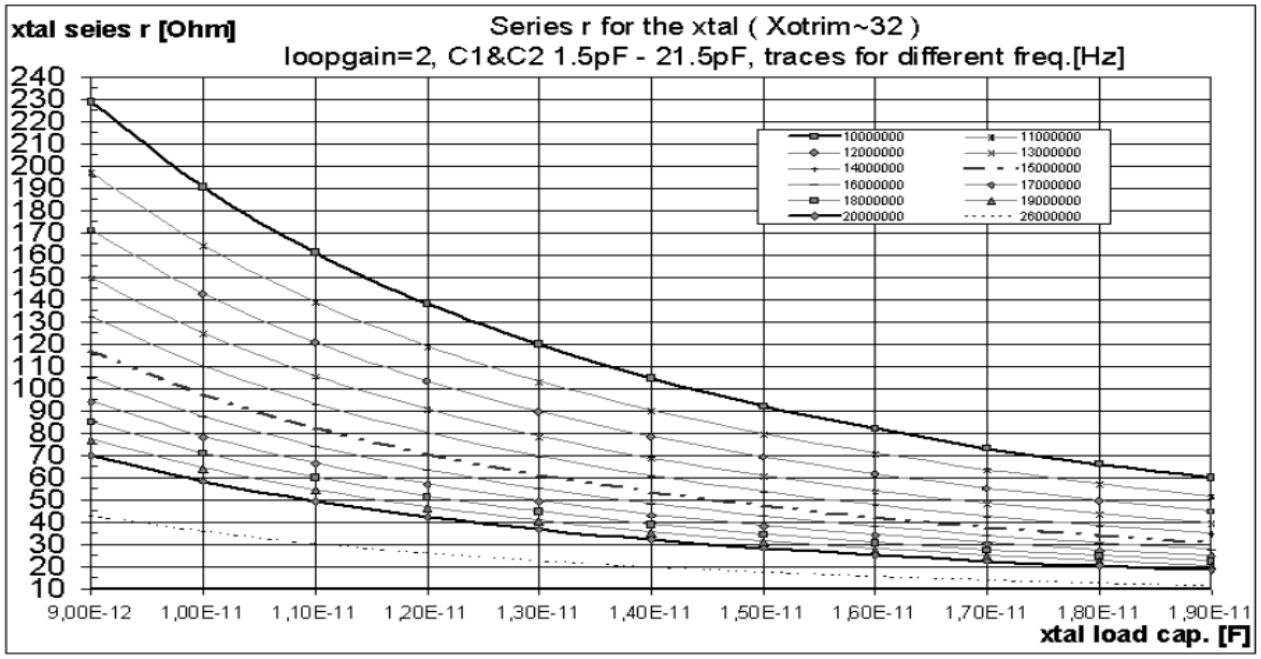

Figure 14. ESR vs. Load capacitance for the crystal circuit

10.0 System Power-Up Sequence

In order to correctly power-up the LMX9820A the following sequence must be performed:

Apply IOVCC and VCC to the LMX9820A.

The Reset_b# and Reset_5100# of the LMX9820A should be driven high minimum of 2ms after the LMX9820A voltage rails are high. The LMX9820A is properly reset.

Reference Table 29 on page 23.

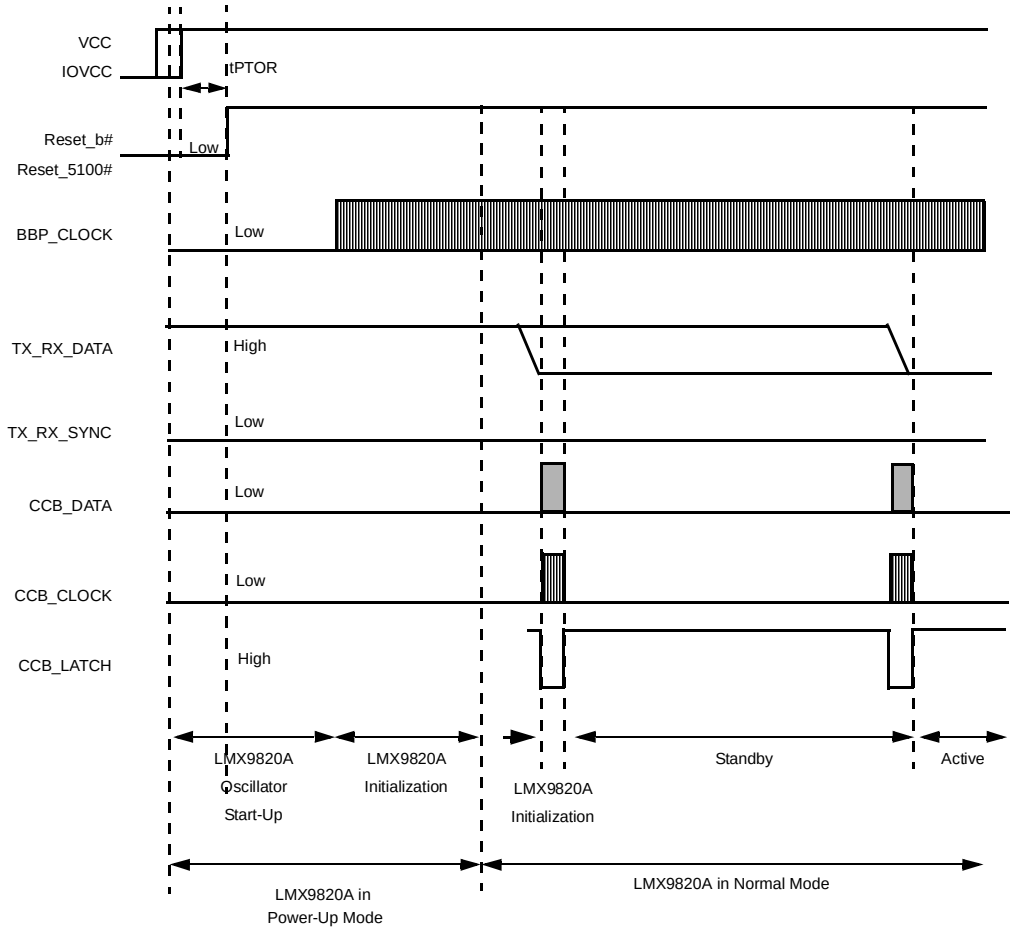

Figure 15. LMX9820A System Power-Up Sequence Timing

Table 29. LMX9820A System Power-up Sequence Timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{PTOR}	Power to Reset	V_{CC} and IO_{VCC} at operating voltage level to valid reset	2			ms

11.0 Integrated Firmware

The LMX9820A includes the full Bluetooth stack up to RFComm to support the following profiles:

- GAP (Generic Access Profile)
- SDAP (Service Discovery Application Profile)
- SPP (Serial Port Profile)

Figure 16 shows the Bluetooth protocol stack with command interpreter interface. The command interpreter offers a number of different commands to support the functionality given by the different profiles. Execution and interface timing is handled by the control application.

The chip has an internal data area in Flash that includes the parameters shown in Table 30 on page 25.

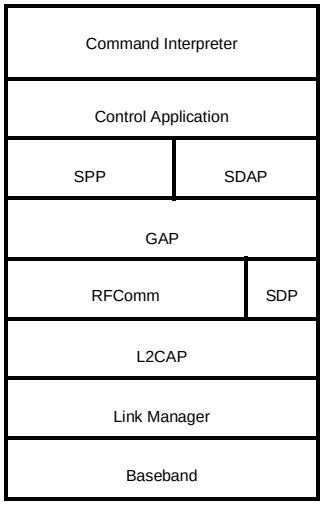

Figure 16. LMX9820A Software Implementation

11.1 .FEATURES

11.1.1 Operation Modes

On boot-up, the application configures the module following the parameters in the data area.

Automatic Mode

No Default Connections Stored:

In Automatic mode the module is connectable and discoverable and automatically answers to service requests. The command interpreter listens to commands and links can be set up. The full command list is supported.

If connected by another device, the module sends an event back to the host, where the RFComm port has been connected, and switches to transparent mode.

Default Connections Stored:

If default connections were stored on a previous session, once the LMX9820A is reset, it will attempt to connect each device stored within the data Flash three times. The host will be notified about the success of the link setup via a link status event.

Command Mode

In Command mode, the LMX9820A does not check the default connections section within the Data Flash. If connected by another device, it will NOT switch to transparent mode and continue to interpret data sent on the UART.

Transparent Mode

The LMX9820A supports transparent data communication from the UART interface to a bluetooth link.

If activated, the module does not interpret the commands on the UART which normally are used to configure and control the module. The packages don't need to be formatted as described in Table 32 on page 27. Instead all data are directly passed through the firmware to the active bluetooth link and the remote device.

Transparent mode can only be supported on a point-to-point connection. To leave Transparent mode, the host must send a UART_BREAK signal to the module

Force Master Mode

In Force Master mode tries to act like an Accesspoint for multiple connections. For this it will only accept the link if a Master/slave role switch is accepted by the connecting device. After successful link establishment the LMX9820A will be Master and available for additional incoming links. On the first incoming link the LMX9820A will switch to transparent depending on the setting for automatic or command mode. Additional links will only be possible if the device is not in transparent mode.

11.1.2 Default Connections

The LMX9820A supports the storage of up to 3 devices within its NVS. Those connections can either be connected after reset or on demand using a specific command.

11.1.3 Event Filter

The LMX9820A uses events or indicators to notify the host about successful commands or changes at the bluetooth interface. Depending on the application the LMX9820A can be configured. The following levels are defined:

- No Events:
  - The LMX9820A is not reporting any events. Optimized for passive cable replacement solutions.
- Standard LMX9820A events:
  - only necessary events will be reported
- All events:
  - Additional to the standard all changes at the physical layer will be reported.

11.1.4 Default Link Policy

Each Bluetooth Link can be configured to support M/S role switch, Hold Mode, Sniff Mode and Park Mode. The default link policy defines the standard setting for incoming and outgoing connections.

Table 30. Operation Parameters Stored in LMX9820A

Parameter	Default Value	Description
BDADDR	(Hard coded into Device)	Bluetooth device address
Local Name	Serial port device	
PinCode	0000	Bluetooth PinCode
Operation Mode	Automatic	Command or Automatic mode
Default Connections	0	Up to three default devices to connect on default
SDP Database	1 SPP entry: Name: COM1 Authentication and encryption enabled	Service discovery database, control for supported profiles
UART Speed	9600	Sets the speed of the physical UART interface to the host
UART Settings	1 Stop bit, parity disabled	Parity and stop bits on the hardware UART interface
Ports to Open	0000 0001	Defines the RFComm ports to open
Link Keys	No link keys	Link keys for paired devices
Security Mode	2	Security mode
Page Scan Mode	Connectable	Connectable/Not connectable for other devices
Inquiry Scan Mode	Discoverable	Discoverable/Not Discoverable/Limited Discoverable for other devices
Default Link Policy	All modes allowed	Configures modes allowed for incoming or outgoing connections (Role switch, Hold mode, Sniff mode, Park mode)
Event Filter	Standard LMX9820A events reported	Defines the level of reporting on the UART - no events - standard events - standard including ACL link events

12.0 Low Power Modes (Continued)

12.0 Low Power Modes

The LMX9820A supports different Low Power Modes to reduce power in different operating situations. The modular structure of the LMX9820A allows the firmware to power down unused modules.

The Low power modes have influence on:

- UART transport layer
  - enabling or disabling the interface
- Bluetooth Baseband activity
  - firmware disables LLC and Radio if possible

12.1 POWER MODES

The following LMX9820A power modes, which depend on the activity level of the UART transport layer and the radio activity are defined:

The radio activity level mainly depends on application requirements and is defined by standard bluetooth operations like inquiry/page scanning or an active link.

A remote device establishing or disconnecting a link may also indirectly change the radio activity level.

The UART transport layer by default is enabled on device power up. In order to disable the transport layer the command “Disable Transport Layer” is used. Thus only the Host side command interface can disable the transport layer. Enabling the transport layer is controlled by the HW Wakeup signalling. This can be done from either the Host and the LMX9820A. See also “LMX9820A Software Users Guide” for detailed information on timing and implementation requirements.

Table 31. Power Mode activity

Power Mode	UART activity	Radio activity	Reference Clock
PM0	OFF	OFF	32.768kHz
PM1	ON	OFF	12MHz
PM2	OFF	Scanning	12MHz/32.768 kHz
PM3	ON	Scanning	12MHz
PM4	OFF	SPP Link	12MHz
PM5	ON	SPP Link	12MHz

12.2 ENABLING AND DISABLING UART TRANSPORT

12.2.1 Hardware Wake up functionality

In certain usage scenarios the host is able to switch off the transport layer of the LMX9820A in order to reduce power consumption. Afterwards both devices, host and LMX9820A are able to shut down their UART interfaces.

In order to save system connections the UART interface is reconfigured to hardware wakeup functionality. For a detailed timing and command functionality please see also the “LMX9820A Software Users Guide”.

The interface between host and LMX9820A is defined as described in Figure 17.

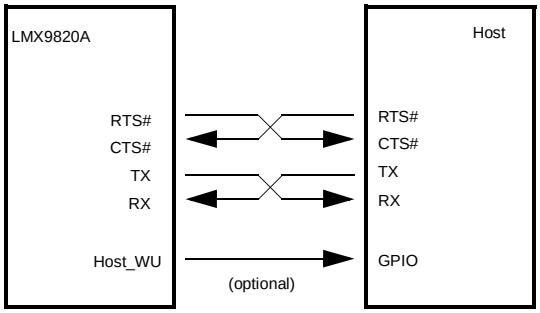

Figure 17. UART NULL modem connection

12.2.2 Disabling the UART transport layer

The Host can disable the UART transport layer by sending the “Disable Transport Layer” Command. The LMX9820A will empty its buffers, send the confirmation event and disable its UART interface. Afterwards the UART interface will be reconfigured to wake up on a falling edge of the CTS pin.

12.2.3 LMX9820A enabling the UART interface

As the Transport Layer can be disabled in any situation the LMX9820A must first make sure the transport layer is enabled before sending data to the host. Possible scenarios can be incoming data or incoming link indicators. If the UART is not enabled the LMX9820A assumes that the Host is sleeping and waking it up by activating RTS and setting HOST_WU to 1. To be able to react on that Wake up, the host has to monitor the CTS pin.

As soon as the host activates its RTS pin, the LMX9820A will first send a confirmation event and then start to transmit the events.

12.2.4 Enabling the UART transport layer from the host

If the host needs to send data or commands to the LMX9820A while the UART Transport Layer is disabled it must first assume that the LMX9820A is sleeping and wake it up using its RTS signal.

When the LMX9820A detects the Wake-Up signal it activates the UART HW and acknowledges the Wake-Up signal by settings its RTS and HOST_WU signal. Additionally the Wake up will be confirmed by a confirmation event. When the Host has received this “Transport Layer Enabled” event, the LMX9820A is ready to receive commands.

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13.0 Command Interface

The LMX9820A offers Bluetooth functionality in either a self contained slave functionality or over a simple command interface. The interface is listening on the UART interface.

The following sections describe the protocol transported on the UART interface between the LMX9820A and the host in command mode (see Figure 18). In Transparent mode, no data framing is necessary and the device does not listen for commands.

13.1 FRAMING

The connection is considered “Error free”. But for packet recognition and synchronization, some framing is used.

All packets sent in both directions are constructed per the model shown in Table 32.

13.1.1 Start and End Delimiter

The “STX” char is used as start delimiter: STX = 0x02. ETX = 0x03 is used as end delimiter.

13.1.2 Packet Type ID

This byte identifies the type of packet. See Table 33 for details.

13.1.3 Opcode

The opcode identifies the command to execute. The opcode values can be found within the “LMX9820A Software User’s Guide” included within the LXMX9820 Evaluation Board.

13.1.4 Data Length

Number of bytes in the Packet Data field. The maximum size is defined with 333 data bytes per packet.

13.1.5 Checksum:

This is a simple Block Check Character (BCC) checksum of the bytes “Packet type”, “Opcode” and “Data Length”. The BCC checksum is calculated as low byte of the sum of all bytes (e.g., if the sum of all bytes is 0x3724, the checksum is 0x24).

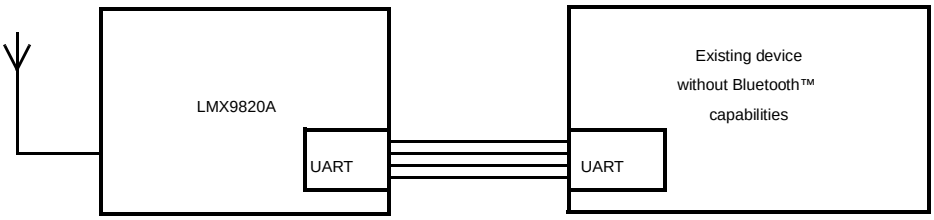

Figure 18. Bluetooth Functionality

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Table 32. Package Framing

Start Delimiter	Packet Type ID	Opcode	Data Length	Checksum	Packet Data	End Delimiter
1 Byte	1 Byte	1 Byte	2 Bytes	1 Byte	<Data Length> Bytes	1 Byte
	- - - - - - - - - - - - - Checksum - - - - - - - - - - - - -					

Table 33. Packet Type Identification

ID	Direction	Description
0x52 ‘R’	REQUEST (REQ)	A request sent to the Bluetooth module. All requests are answered by exactly one confirm.
0x43 ‘C’	Confirm (CFM)	The Bluetooth modules confirm to a request. All requests are answered by exactly one confirm.
0x69 ‘i’	Indication (IND)	Information sent from the Bluetooth module that is not a direct confirm to a request. Indicating status changes, incoming links, or unrequested events.
0x72 ‘r’	Response (RES)	An optional response to an indication. This is used to respond to some type of indication message.

13.0 Command Interface (Continued)

13.2 COMMAND SET OVERVIEW

The LMX9820A has a well defined command set to:

- Configure the device:
  - Hardware settings
  - Local Bluetooth parameters
  - Service database
- Set up and handle links

Tables 34 through 43 show the actual command set and the events coming back from the device. A full documented description of the commands can be found in the "LMX9820A Software Users Guide".

NOTE: For standard Bluetooth operation only commands from Table 34 through Table 36 will be used. Most of the remaining commands are for configuration purposes only.

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Table 34. Device Discovery

Command	Event	Description
Inquiry	Inquiry Complete	Search for devices
	Device Found	Lists BDADDR and class of device
Remote Device Name	Remote Device Name Confirm	Get name of remote device

Table 35. SDAP Client Commands

Command	Event	Description
SDAP Connect	SDAP Connect Confirm	Create an SDP connection to remote device
SDAP Disconnect	SDAP Disconnect Confirm	Disconnect an active SDAP link
	Connection Lost	Notification for lost SDAP link
SDAP Service Browse	Service Browse Confirm	Get the services of the remote device
SDAP Service Search	SDAP Service Search Confirm	Search a specific service on a remote device
SDAP Attribute Request	SDAP Attribute Request Confirm	Searches for services with specific attributes

Table 36. SPP Link Establishment

Command	Event	Description
Establish SPP Link	Establishing SPP Link Confirm	Initiates link establishment to a remote device
	Link Established	Link successfully established
	Incoming Link	A remote device established a link to the local device
Release SPP Link	Release SPP Link Confirm	Initiate release of SPP link
SPP Send Data	SPP Send Data Confirm	Send data to specific SPP port
	Incoming Data	Incoming data from remote device
Transparent Mode	Transparent Mode Confirm	Switch to Transparent mode on the UART

Table 37. Storing Default Connections

Command	Event	Description
Connect Default Connection	Connect Default Connection Confirm	Connects to either one or all stored default connections
Store Default Connection	Store Default Connection Confirm	Store device as default connection

Table 37. Storing Default Connections

Command	Event	Description
Get list of Default Connections	List of Default Devices	
Delete Default Connections	Delete Default Connections Confirm	

Table 38. Bluetooth Low Power Modes

Command	Event	Description
Set Default Link Policy	Set Default Link Policy Confirm	Defines the link policy used for any incoming or outgoing link.
Get Default Link Policy	Get Default Link Policy Confirm	Returns the stored default link policy
Set Link Policy	Set Link Policy Confirm	Defines the modes allowed for a specific link
Get Link Policy	Get Link Policy Confirm	Returns the actual link policy for the link
Enter Sniff Mode	Enter Sniff Mode Confirm	
Exit Sniff Mode	Exit Sniff Mode Confirm	
Enter Park Mode	Enter Park Mode Confirm	
Enter Hold Mode	Enter Hold Mode Confirm	
	Power Save Mode Changed	Remote device changed power save mode on the link

Table 39. Wake Up Functionality

Command	Event	Description
Disable Transport Layer	Transport Layer Enabled	Disabling the UART Transport Layer and activates the Hardware Wakeup function

Table 40. SPP Port Configuration and Status

Command	Event	Description
Set Port Config	Set Port Config Confirm	Set port setting for the “virtual” serial port link over the air
Get Port Config	Get Port Config Confirm	Read the actual port settings for a “virtual” serial port
	Port Config Changed	Notification if port settings were changed from remote device
SPP Get Port Status	SPP Get Port Status Confirm	Returns status of DTR, RTS (for the active RFComm link)
SPP Port Set DTR	SPP Port Set DTR Confirm	Sets the DTR bit on the specified link
SPP Port Set RTS	SPP Port Set RTS Confirm	Sets the RTS bit on the specified link
SPP Port BREAK	SPP Port BREAK	Indicates that the host has detected a break
SPP Port Overrun Error	SPP Port Overrun Error Confirm	Used to indicate that the host has detected an overrun error
SPP Port Parity Error	SPP Port Parity Error Confirm	Host has detected a parity error
SPP Port Framing Error	SPP Port Framing Error Confirm	Host has detected a framing error
	SPP Port Status Changed	Indicates that remote device has changed one of the port status bits

13.0 Command Interface (Continued)

Table 41. Local Bluetooth Settings

Command	Event	Description
Read Local Name	Read Local Name Confirm	Read actual friendly name of the device
Write Local Name	Write Local Name Confirm	Set the friendly name of the device
Read Local BDADDR	Read Local BDADDR Confirm	
Change Local BDADDR	Change Local BDADDR Confirm	**Note:** Only use if you have your own BDADDR pool
Store Class of Device	Store Class of Device Confirm	
Set Scan Mode	Set Scan Mode Confirm	Change mode for discoverability and connectability
	Set Scan Mode Indication	Reports end of Automatic limited discoverable mode
Get Fixed Pin	Get Fixed Pin Confirm	Reads current PinCode stored within the device
Set Fixed Pin	Set Fixed Pin Confirm	Set the local PinCode
Get Security Mode	Get Security Mode Confirm	Get actual Security mode
Set Security Mode	Set Security Mode Confirm	Configure Security mode for local device (default 2)
Remove Pairing	Remove Pairing Confirm	Remove pairing with a remote device
List Paired Devices	List of Paired Devices	Get list of paired devices stored in the LMX9820A data memory
Force Master Role	Force Master Role Confirm	Enables/Disables the request for Master role at incoming connections

Table 42. Local Service Database Configuration

Command	Event	Description
Store SPP Record	Store SPP Record Confirm	Create a new SPP record within the service database
Store DUN Record	Store DUN Record Confirm	Create a new DUN record within the service database
Store FAX Record	Store FAX Record Confirm	Create a new FAX record within the service database
Store OPP Record	Store OPP Record Confirm	Create a new OPP record within the service database
Store FTP Record	Store FTP Record Confirm	Create a new FTP record within the service database
Store IrMCSync Record	Store IrMCSync Record Confirm	Create a new IrMCSync record within the service database
Enable SDP Record	Enable SDP Record Confirm	Enable or disable SDP records
Delete All SDP Records	Delete All SDP Records Confirm	
Ports to Open	Ports to Open Confirmed	Specify the RFComm Ports to open on startup

Table 43. Local Hardware Commands

Command	Event	Description
Set Event Filter	Set Event Filter Confirm	Configures the reporting level of the command interface
Get Event Filter	Get Event Filter Confirm	Get the status of the reporting level
Read RSSI	Read RSSI Confirm	Returns an indicator for the incoming signal strength
Change UART Speed	Change UART Speed Confirm	Set specific UART speed; needs proper ISEL pin setting
Change UART Settings	Change UART Settings Confirm	Change configuration for parity and stop bits
Test Mode	Test Mode Confirm	Enable Bluetooth, EMI test, or local loopback
Restore Factory Settings	Restore Factory Settings Confirm	
Reset	Dongle Ready	Soft reset
Firmware Upgrade		Stops the bluetooth firmware and executes the In-system-programming code

14.0 Usage Scenarios

14.1 SCENARIO 1: POINT-TO-POINT CONNECTION

LMX9820A acts only as slave, no further configuration is required.

Example: Sensor with LMX9820A; hand-held device with standard Bluetooth option.

The SPP conformance of the LMX9820A allows any device using the SPP to connect to the LMX9820A.

Because of switching to Transparent automatically, the controller has no need for an additional protocol layer; data is sent raw to the other Bluetooth device.

On default, a PinCode is requested to block unallowed targeting.

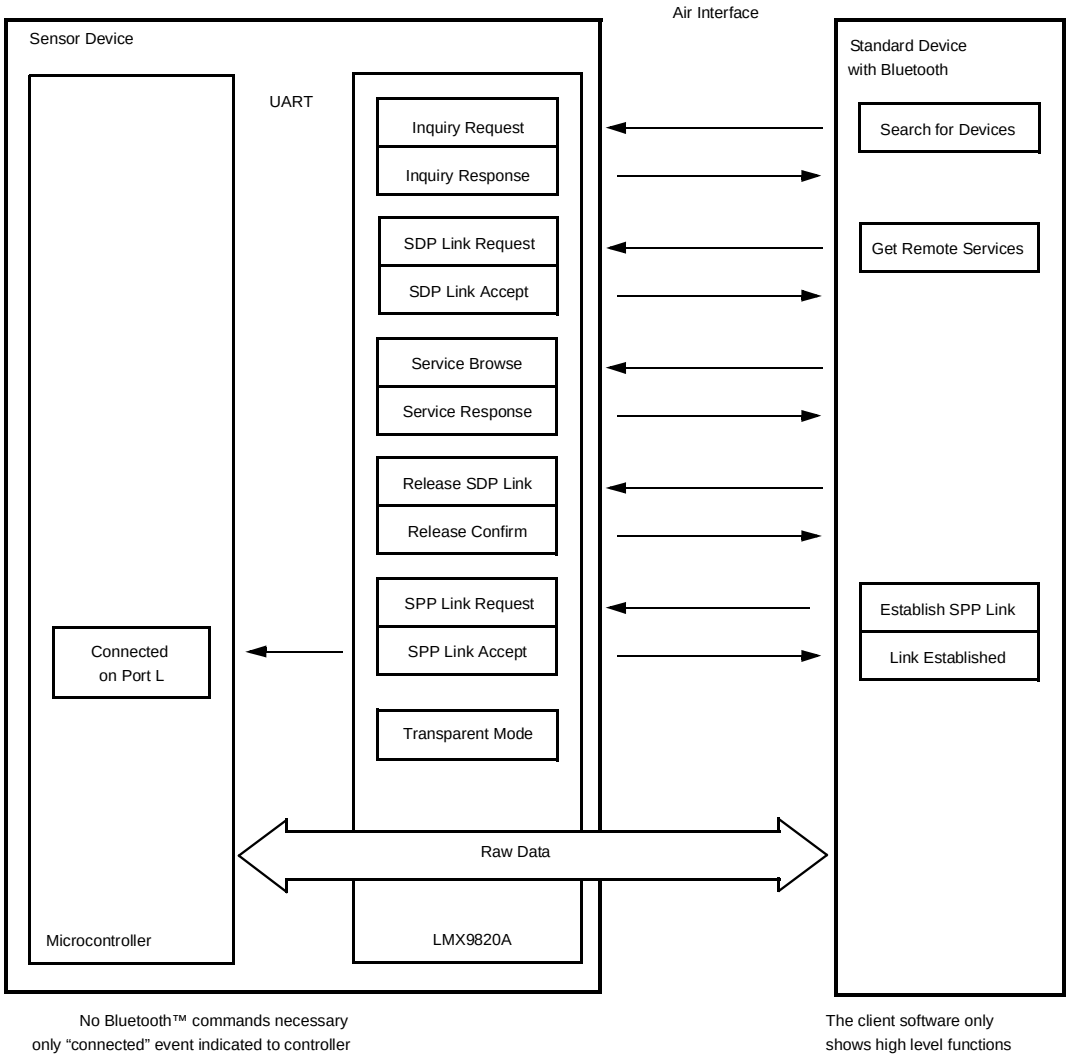


Figure 19. Point-to-Point Connection

14.0 Usage Scenarios (Continued)

14.2 SCENARIO 2: AUTOMATIC POINT-TO-POINT CONNECTION

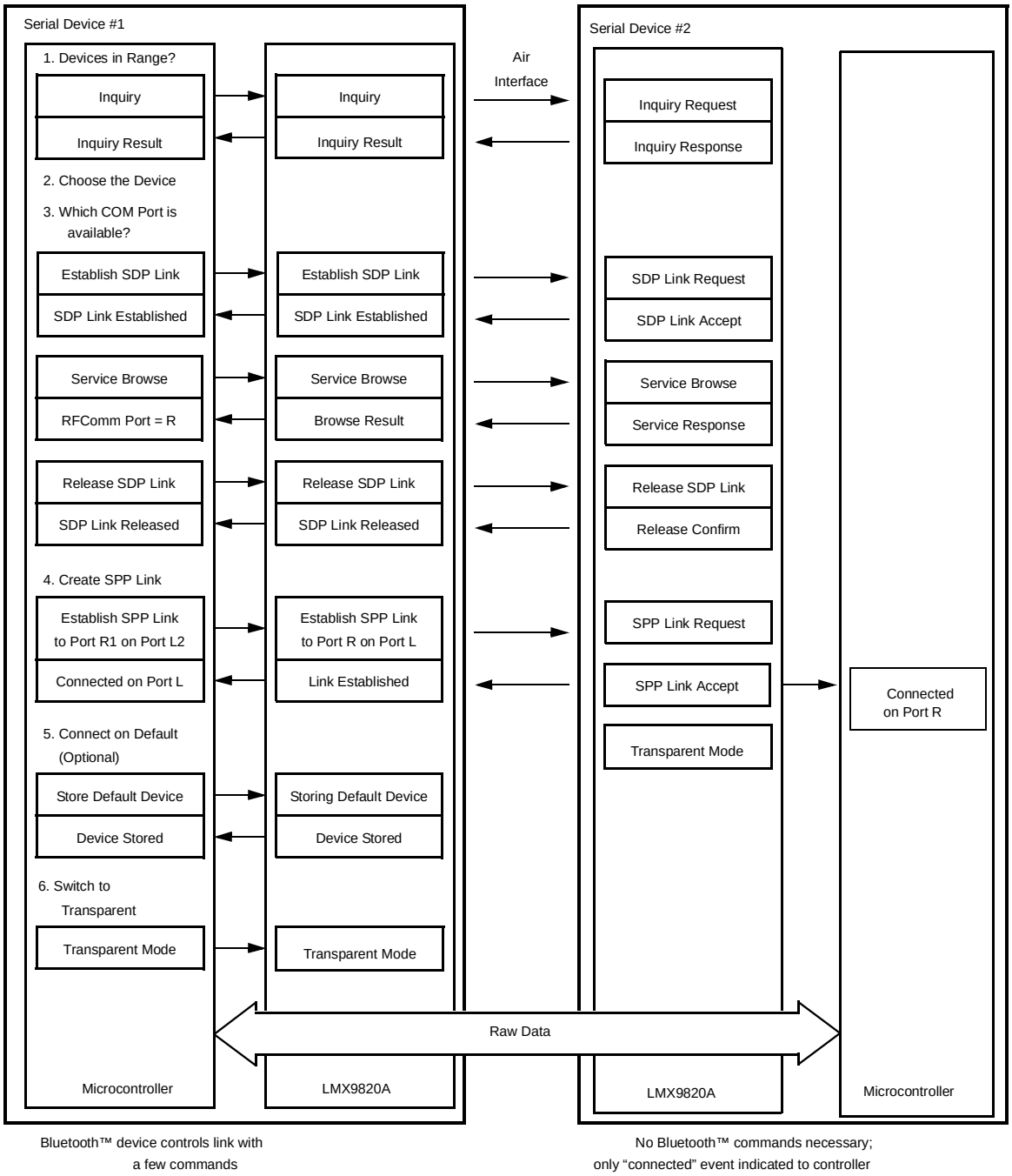
LMX9820A at both sides.

Example: Serial Cable Replacement.

Device #1 controls the link setup with a few commands as described.

If step 5 is executed, the stored default device is connected (step 4) after reset (in Automatic mode only) or by sending the command “Connect to Default Device”. The command can be sent to the device at any time.

If step 6 is left out, the microcontroller has to use the command “Send Data” instead of sending data directly to the module.



1. Port R indicates the remote RFComm channel to connect to. Usually the result of the SDP request.
2. Port L indicates the Local RFComm channel used for that connection.

Figure 20. Automatic Point-to-Point Connection

14.0 Usage Scenarios (Continued)

14.3 SCENARIO 3: POINT-TO-MULTIPOINT CONNECTION

LMX9820A acts as master for several slaves.

Example: Two sensors with LMX9820A; one hand-held device with implemented LMX9820A.

Serial Devices #2 and #3 establish the link automatically as soon as they are contacted by another device. No controller interaction is necessary for setting up the Bluetooth link. Both switch automatically into Transparent mode. The host sends raw data over the UART.

Serial Device #1 is acting as master for both devices. As the host has to decide to or from which device data is coming from, data must be sent using the “Send data command”. If the device receives data from the other devices, it is packaged into an event called “Incoming data event”. The event includes the device related port number.

If necessary, a link configuration can be stored as default in the master Serial Device #1 to enable the automatic reconnect after reset, power-up, or by sending the “connect default connection” command.

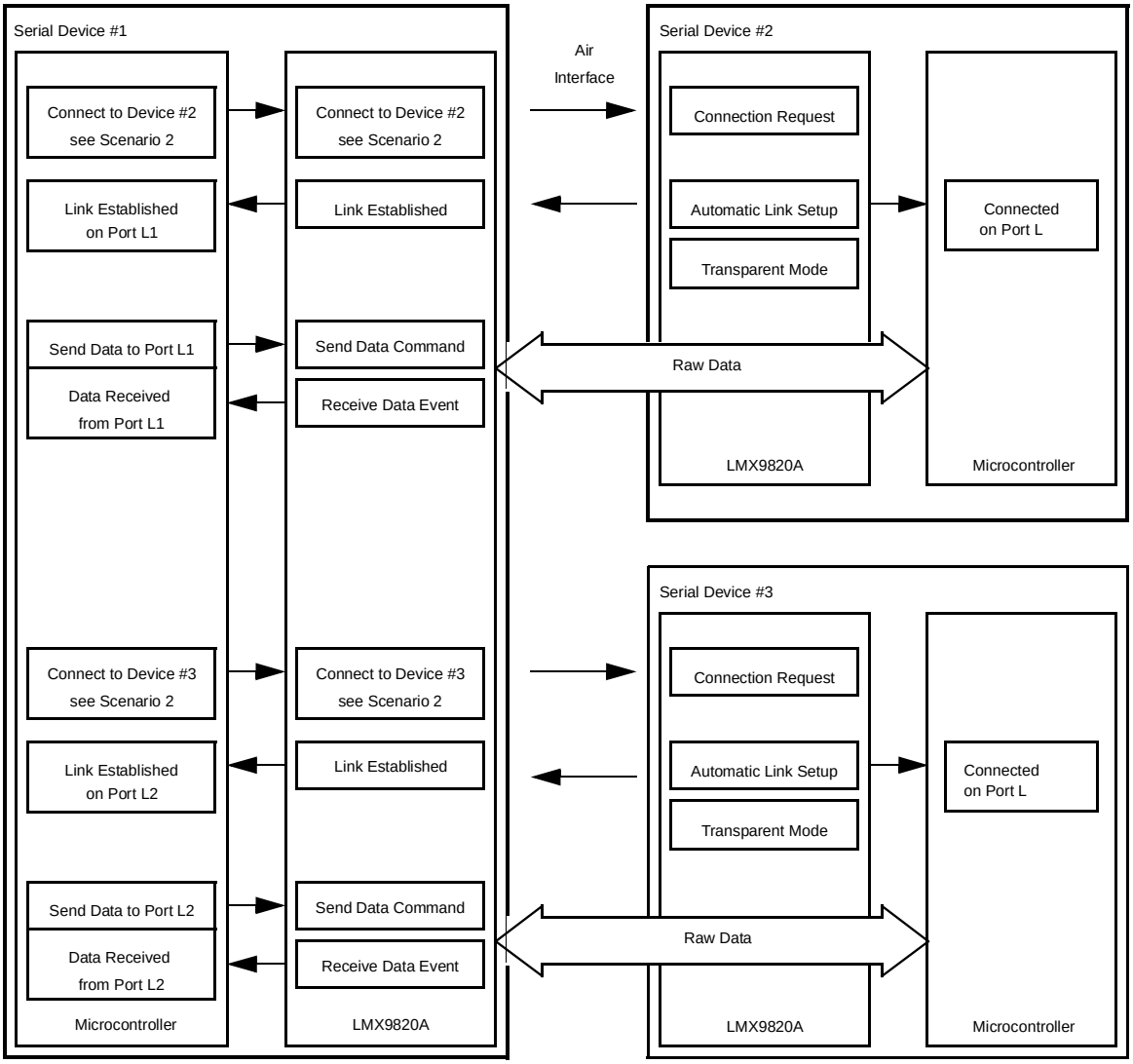


Figure 21. Point-to-Multipoint Connection

15.0 Application Information

Figure 22 on page 35 represents a typical system schematic for the LMX9820A.

15.1 MATCHING NETWORK

The antenna matching network may or may not be required, depending upon the impedance of the antenna chosen. A 6.8pF blocking capacitor is recommended.

15.2 FILTERED POWER SUPPLY

It is imperative that the LMX9820A be provided with adequate Ground planes and a filtered power supply. It is highly recommended that a 0.1 µF and a 10 pF bypass capacitor be placed as close as possible to VCC (pad H2) on the LMX9820A.

15.3 HOST INTERFACE

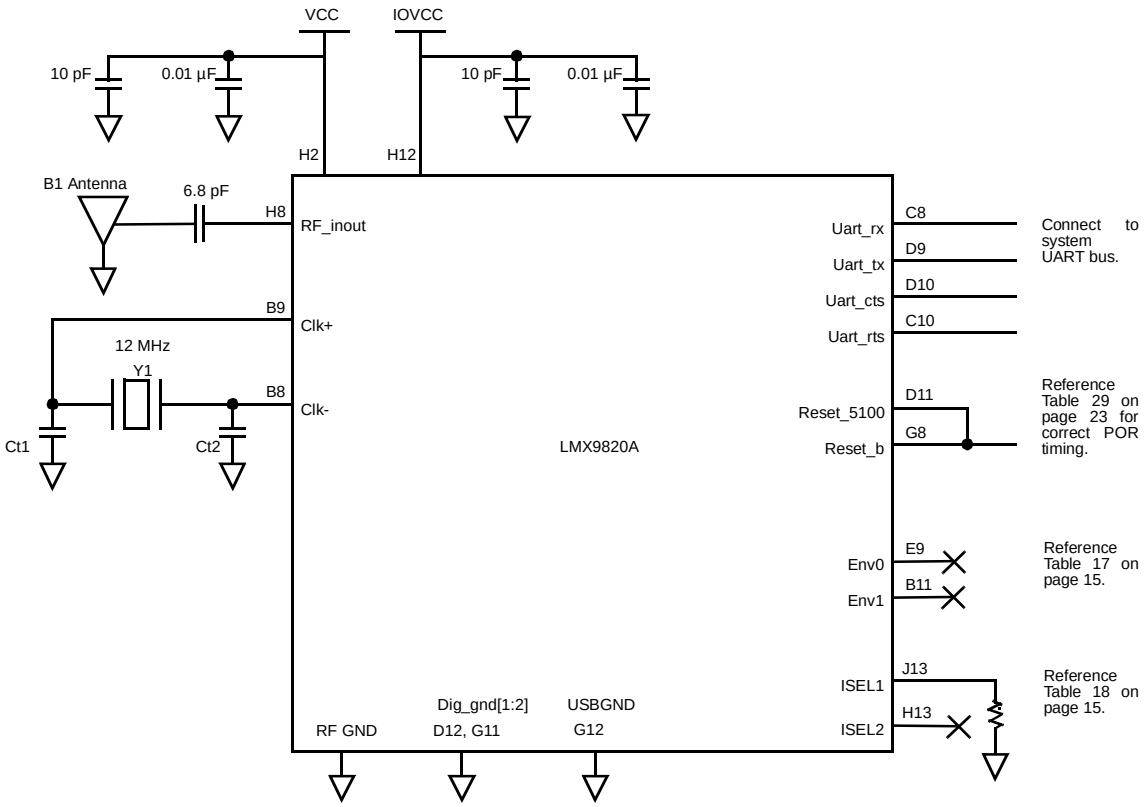
To set the logic thresholds of the LMX9820A to match the host system, IOVCC (pad H12) must be connected to the logic power supply of the host system. It is highly recommended that a 10 pF bypass capacitor be placed as close as possible to the IOVCC pad on the LMX9820A.

ISEL2 (pad H13) and ISEL1 (pad J13) can be strapped to the host logic 0 and 1 levels to set the host interface boot-up configuration. Alternatively both ISEL2 and ISEL1 can be hardwired over 10KΩ pull-up/pull-down resistors.
Env0 (pad E9) and Env1 (pad B11) can be left unconnected (both are read as high) if no ISP capability is required. If the environment mode ISP needs to be activated by hardware (alternatively a firmware upgrade command can be used) then Env0 must be set to Logical Low and Reset needs to be set. Upon removal of Reset, the LMX9820A boots into the mode corresponding to the values present on Env0 and Env1.

15.4 CLOCK INPUT

The clock source must be placed as close as possible to the LMX9820A. The quality of the radio performance is directly related to the quality of the clock source connected to the oscillator port on the LMX9820A. Careful attention must be paid to the crystal/oscillator parameters or radio performance could be drastically reduced.

15.5 SCHEMATIC AND LAYOUT EXAMPLES



Notes:

Capacitor values, Ct1 and Ct2 may vary depending on board design crystal manufacturer specification.

Single ground plane is used for both RF and Digital grounds.

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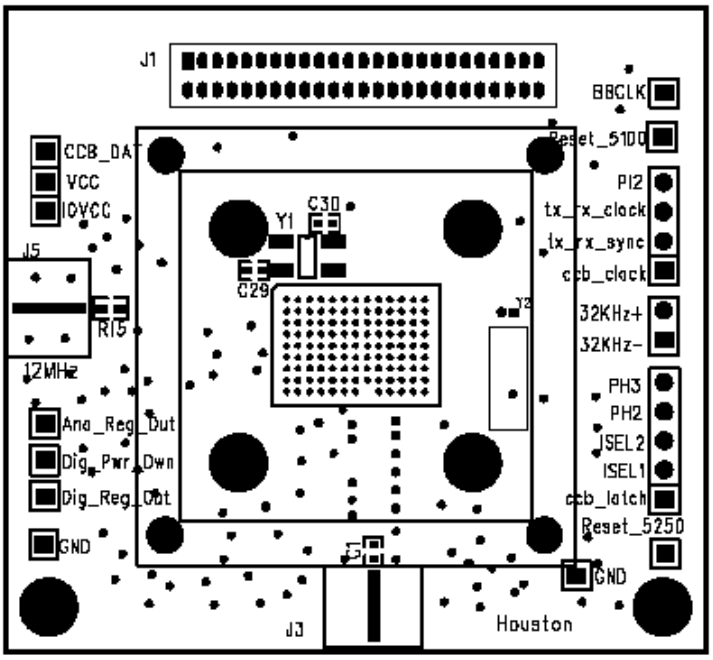
Figure 22. Example System Schematic with pre-selected 115.2kbit/s UART speed



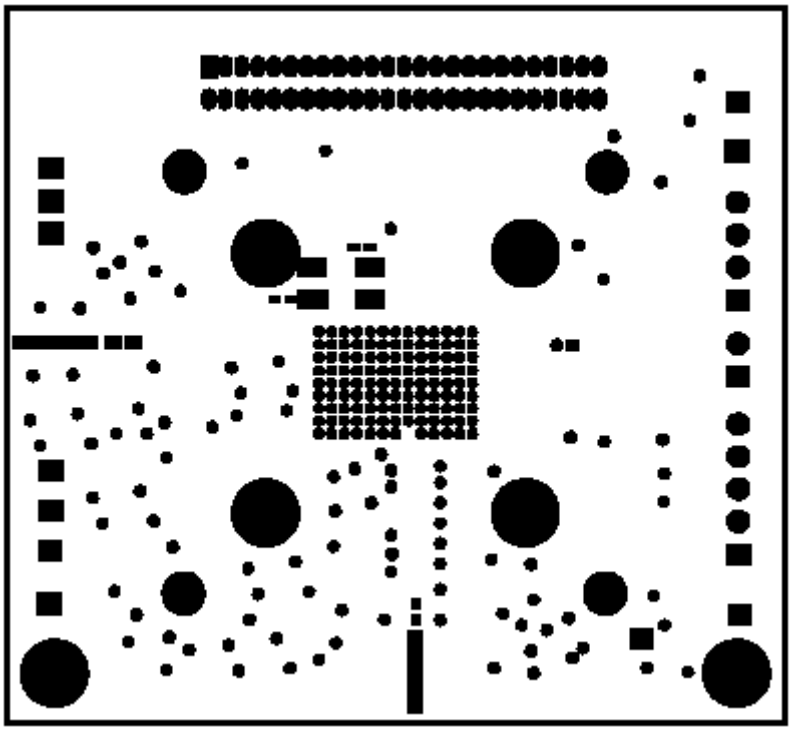


Figure 23. Component Placement - Layer 1

15.0 Application Information (Continued)

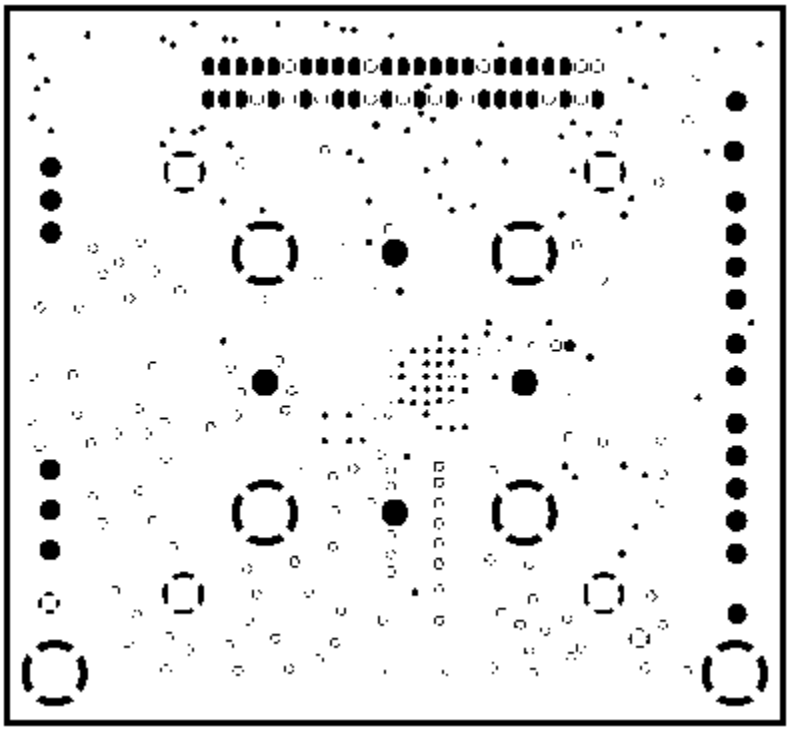


Figure 24. Solid Ground Plane - Layer 2

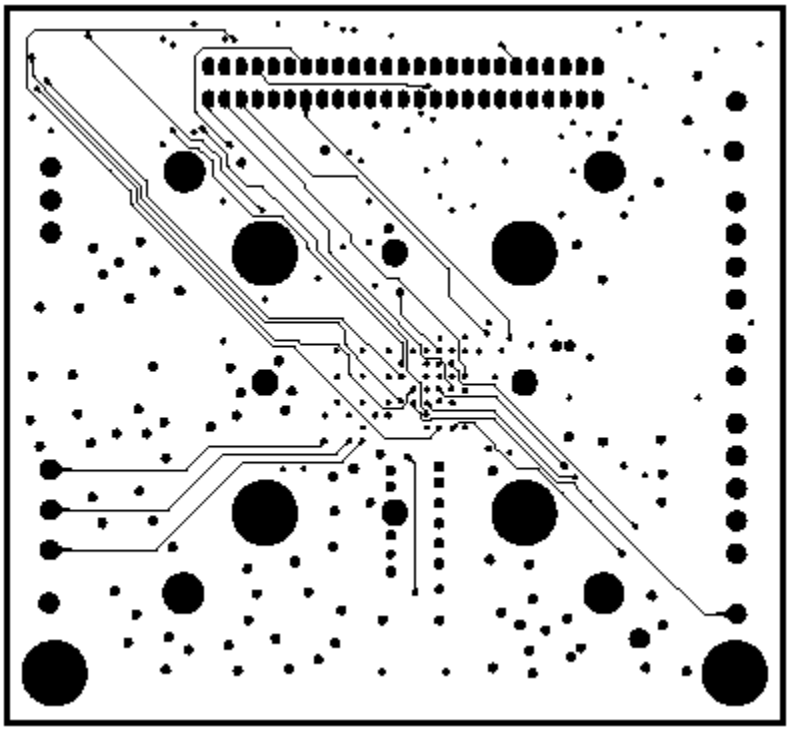


Figure 25. Signal Plane - Layer 3

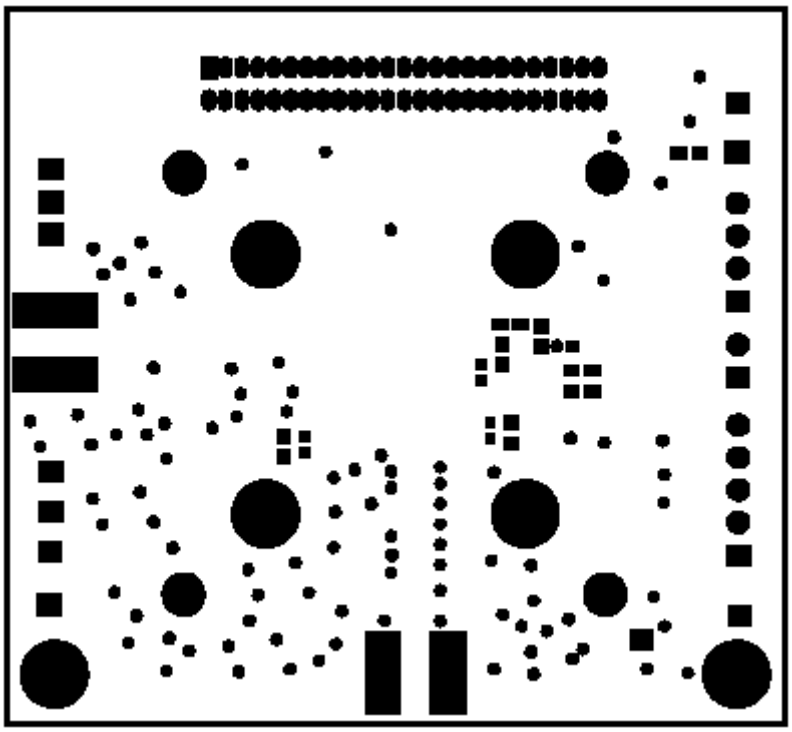


Figure 26. Component Layout Bottom - Layer 4

16.0 Soldering

The LMX9820A bumps are designed to melt as part of the Surface Mount Assembly (SMA) process. The LMX9820A is assembled with a high temperature solder alloy to ensure there are no re-reflow conditions imposed upon the module when reflowed to a PCB with these typical low temperature 60/40 (S = 183°C, L = 188°C), 62/36/2 (E = 179°C), or 63/37 (E = 183°C) solder alloys.

Where:

- S: Solidus
  - Denotes the points in a phase diagram representing the temperature at which the solder composition begins to melt during heating, or complete freezing during cooling.
- L: Liquidus
  - Denotes the points in a phase diagram representing the temperature at which the solder has molten components. The temperature that melting starts at.
- E: Eutectic
  - Denotes solid to liquid without a plastic phase.

The low temperature solder alloy will reflow with the solder bump and provide the maximum allowable solder joint reliability.

Reflow at a peak of 215 --> 220°C (approximately 30 seconds at peak) [not to exceed 225°C; measured in close proximity of the modules] to avoid any potential re-reflow conditions.

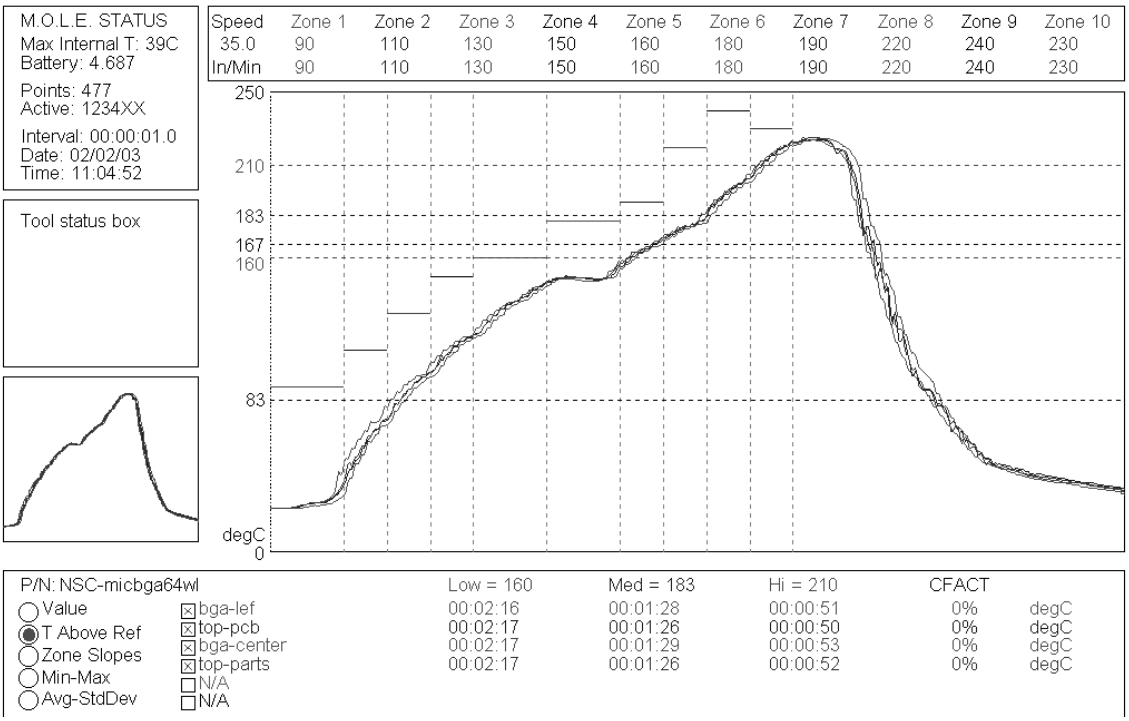
Table 44 and Figure 27 on page 40 provide the soldering details required to properly solder the LMX9820A to standard PCBs. The illustration serves only as a guide and National is not liable if a selected profile does not work.

Table 44. Soldering Details

Parameter	Value
PCB Land Pad Diameter	24 mil
PCB Solder Mask Opening	30 mil
PCB Finish (HASL details)	63/37 (difference in thickness < 28 micron)
Stencil Aperture	28 mil
Stencil Thickness	5 mil
Solder Paste Used	Low temperature 60/40 (S = 183°C, L = 188°C), 62/36/2 (E = 179°C), or 63/37 (E = 183°C) solder alloys[1]
Flux Cleaning Process	No Clean Flux System[1]
Reflow Profiles	See Figure 27 on page 40

1. Typically defined by customer.

16.0 Soldering (Continued)



Profile #	Peak	Min	Max Rising Slope	Max Falling Slope	Rising Time 130	Time Between 130/160	Rising Time 160	Time Between 160/183	Total Time Above 183
1	213.9	32.8	2.50	-1.60	208.01	109.00	99.01	57.00	75.00
2	206.7	31.1	2.41	-1.73	213.01	121.01	92.00	53.00	64.00

Figure 27. Typical Reflow Profiles

17.0 Datasheet Revision History

This section is a report of the revision/creation process of the datasheet for the LMX9820A. Table 45 provides the stages/definitions of the datasheet. Table 46 lists the revision history and Table 47 lists the specific edits to create the current revision.

Table 45. Documentation Status Definitions

Datasheet Status	Product Status	Definition
Advance Information	Formative or in Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data. Supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.S
No Identification Noted	Full production	This datasheet contains final specifications. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not in Production	This datasheet contains specifications on a product that has been discontinued by National Semiconductor Corporation. The datasheet is printed for reference information only.

Table 46. Revision History

Revision # (PDF Date)	Revisions / Comments
0.3 (January 2003)	Third draft of preliminary datasheet. First pass through tech pubs.
0.4 (April 2003)	Datasheet revised to include new radio and additional functionality. Several edits have been made to functional, performance, and electrical details.
0.6 (February 2004)	Updated RF performance values Added 32kHz frequency support. See table Table 47 "Edits to Current Revision" on page 42.

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Tel: 81-3-5639-7560

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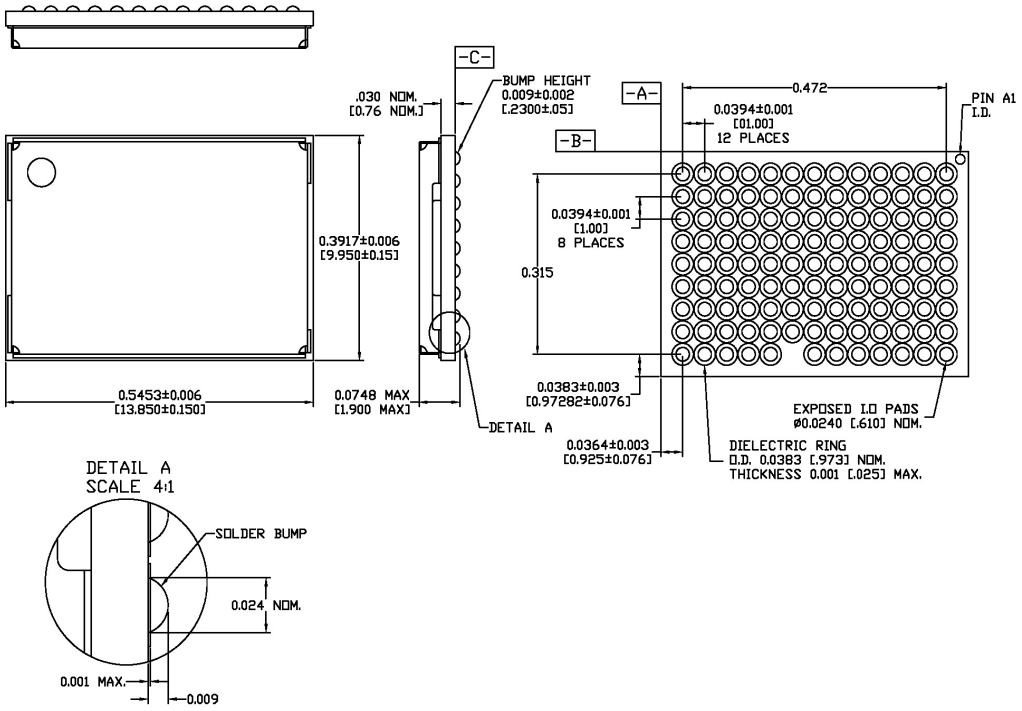
17.0 Datasheet Revision History (Continued)

Table 47. Edits to Current Revision

Section	Revisions / Comments
General Description	
Pad Description	–
Electrical Specifications	•
Functional Description	•
Digital Smart Radio	•
System Power Up Sequence	•
Integrated Firmware	•
Low Power Modes	•
Command Interface	•
Application| Information	•
Soldering	•

18.0 Physical Dimensions inches (millimeters) unless otherwise noted. (Continued)

18.0 Physical Dimensions inches (millimeters) unless otherwise noted.



UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE IN INCHES.

TOLERANCE, UNLESS OTHERWISE SPECIFIED:
TWO PLACE (.00): ±.01
THREE PLACE (.000): ±.002
ANGULAR: ±1°

Figure 28. FR4 Package