CC2500
Single Chip Low Cost Low Power RF-Transceiver

Applications

- *2400-2483.5MHz ISM/SRD band systems*
- *Consumer Electronics*
- *Wireless game controllers*
- *Wireless audio*
- *Wireless keyboard and mouse*

Product Description

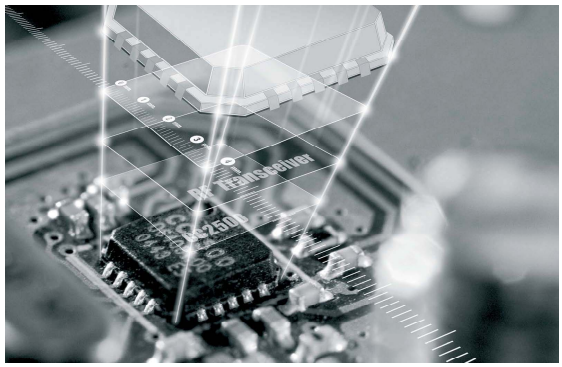
The ***CC2500*** is a low cost true single chip 2.4GHz transceiver designed for very low power wireless applications. The circuit is intended for the ISM (Industrial, Scientific and Medical) and SRD (Short Range Device) frequency band at 2400MHz-2483.5MHz.

The RF transceiver is integrated with a highly configurable baseband modem which has a configurable data rate up to 500kbps. Performance can be increased by enabling a Forward Error Correction option, which is integrated in the modem.

CC2500 provides extensive hardware support for packet handling, data buffering, burst transmissions, clear channel assessment, link quality indication and wake on radio.

The main operating parameters and the 64-byte transmit/receive FIFOs of ***CC2500*** can be controlled via an SPI interface. In a typical system, the ***CC2500*** will be used together with a microcontroller and a few extra passive components.

CC2500 is based on Chipcon's SmartRF®04 technology in 0.18μm CMOS.



Key Features

- Small size (QLP 4x4mm package, 20 pins)
- True single chip 2.4GHz RF transceiver
- Frequency range: *2400MHz-2483.5MHz*
- High sensitivity (–98dBm at 10kbps, 1% packet error rate)
- Programmable data rate up to 500kbps
- Low current consumption (15.6mA in RX)
- Programmable output power up to +1dBm
- Excellent receiver selectivity and blocking performance
- Very few external components: Totally on-chip frequency synthesizer, no external filters or RF switch needed
- Programmable baseband modem
- Ideal for multi-channel operation
- Configurable packet handling hardware
- Suitable for frequency hopping systems due to a fast settling frequency synthesizer
- Optional Forward Error Correction with interleaving
- Separate 64-byte RX and TX data FIFOs
- Efficient SPI interface: All registers can be programmed with one "burst" transfer
- Digital RSSI output
- Suited for systems compliant with EN 300 328 and EN 300 440 class 2 (Europe), CFR47 Part 15 (US), and ARIB STD-T66 (Japan)
- Wake-on-radio functionality for automatic low-power RX polling
- Many powerful digital features allow a high-performance RF system to be made using an inexpensive microcontroller
- Integrated analog temperature sensor
- Lead-free "green" package

Features (continued from front page)

- Flexible support for packet oriented systems: On chip support for sync word detection, address check, flexible packet length and automatic CRC handling.
- Programmable channel filter bandwidth
- OOK and flexible ASK shaping supported
- 2-FSK and MSK supported
- Automatic Frequency Compensation can be used to align the frequency synthesizer to received centre frequency
- Optional automatic whitening and de-whitening of data
- Support for asynchronous transparent receive/transmit mode for backwards compatibility with existing radio communication protocols
- Programmable Carrier Sense indicator
- Programmable Preamble Quality Indicator for detecting preambles and improved protection against sync word detection in random noise
- Support for automatic Clear Channel Assessment (CCA) before transmitting (for listen-before-talk systems)
- Support for per-package Link Quality Indication

1 Abbreviations

Abbreviations used in this data sheet are described below.

2-FSK	Binary Frequency Shift Keying
ADC	Analog to Digital Converter
AFC	Automatic Frequency Offset Compensation
AGC	Automatic Gain Control
AMR	Automatic Meter Reading
ASK	Amplitude Shift Keying
BER	Bit Error Rate
CCA	Clear Channel Assessment
CRC	Cyclic Redundancy Check
ESR	Equivalent Series Resistance
FEC	Forward Error Correction
FSK	Frequency Shift Keying
IF	Intermediate Frequency
LNA	Low Noise Amplifier
LQI	Link Quality Indicator
MCU	Microcontroller Unit
MSK	Minimum Shift Keying
PA	Power Amplifier
PD	Power Down
PER	Packet Error Rate
PLL	Phase Locked Loop
PQI	Preamble Quality Indicator
QPSK	Quadrature Phase Shift Keying
RCOSC	RC Oscillator
RF	Radio Frequency
RSSI	Received Signal Strength Indicator
RX	Receive, Receive Mode
SNR	Signal to Noise Ratio
SPI	Serial Peripheral Interface
TBD	To Be Defined
TX	Transmit, Transmit Mode
VCO	Voltage Controlled Oscillator
WOR	Wake on Radio, Low power polling
XOSC	Crystal Oscillator
XTAL	Crystal

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2 Absolute Maximum Ratings

Under no circumstances must the absolute maximum ratings given in Table 1 be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Caution! *ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.*

Parameter	Min	Max	Units	Condition
Supply voltage	–0.3	3.6	V	All supply pins must have the same voltage
Voltage on any digital pin	–0.3	VDD+0.3, max 3.6	V	
Voltage on the pins RF_P, RF_N and DCOUPL	–0.3	2.0	V	
Input RF level		TBD	dBm	
Storage temperature range	–50	150	°C	
Solder reflow temperature		260	°C	T = 10 s
ESD		2	kV	All pads (excluding RF) have 2kV HBM ESD protection

Table 1: Absolute Maximum Ratings

3 Operating Conditions

The operating conditions for ***CC2500*** are listed Table 2 in below.

Parameter	Min	Max	Unit	Condition
Operating temperature	–40	85	°C	
Operating supply voltage	1.8	3.6	V	All supply pins must have the same voltage

Table 2: Operating Conditions

4 Electrical Specifications

Tc = 25°C, VDD = 3.0V if nothing else stated. Measured on Chipcon's ***CC2500*** EM reference design.

Parameter	Min	Typ	Max	Unit	Condition
Current consumption		8.7		μA	Automatic RX polling once each second, using low-power RC oscillator, with 460Hz filter bandwidth and 250kbps data rate, PLL calibration every 4th wakeup. Average current with signal in channel *below* carrier sense level.
		35		μA	Same as above, but with signal in channel *above* carrier sense level, 1.9ms RX timeout, and no preamble/sync word found.
		1.4		μA	Automatic RX polling every 15th second, using low-power RC oscillator, with 460kHz filter bandwidth and 250kbps data rate, PLL calibration every 4th wakeup. Average current with signal in channel below carrier sense level.
		16		μA	Same as above, but with signal in channel *above* carrier sense level, 14ms RX timeout, and no preamble/sync word found.
		1.8		mA	Only voltage regulator to digital part and crystal oscillator running (IDLE state)
		7.6		mA	Only the frequency synthesizer running (after going from IDLE until reaching RX or TX states, and frequency calibration states)
		15.6		mA	Receive mode, input near sensitivity limit (RX state)
		13.3		mA	Receive mode, input 30dB above sensitivity limit (RX state)
		11.5		mA	Transmit mode, –12dBm output power (TX state)
		15.4		mA	Transmit mode, -6dBm output power (TX state)
		21.6		mA	Transmit mode, 0dBm output power (TX state)
Current consumption in power down modes		180		μA	Voltage regulator to digital part on, all other modules in power down (XOFF state)
		100		μA	Voltage regulator to digital part off, register values retained, XOSC running (SLEEP state with `MCSM0.OSC_FORCE_ON` set)
		900		nA	Voltage regulator to digital part off, register values retained, low-power RC oscillator running (SLEEP state with WOR enabled)
		500		nA	Voltage regulator to digital part off, register values retained (SLEEP state)

Table 3: Electrical Specifications

5 General Characteristics

Parameter	Min	Typ	Max	Unit	Condition/Note
Frequency range	2400		2483.5	MHz	
Data rate	1.2		500	kbps	Modulation formats supported: (Shaped) MSK (differential offset QPSK, up to 500kbps) 2-FSK (up to 250kbps) OOK/ASK (up to 250kbps) Optional Manchester encoding (halves the data rate).

Table 4: General Characteristics

6 RF Receive Section

Tc = 25°C, VDD = 3.0V if nothing else stated. Measured on Chipcon's ***CC2500*** EM reference design.

Parameter	Min	Typ	Max	Unit	Condition/Note
Differential input impedance		200		Ω	Optimised for matching to both 50Ω single-ended load and PCB antennas with higher impedance.
Receiver sensitivity		TBD		dBm	500kbps data rate (MSK), 1% packet error rate, 16 bytes packet length, 650kHz digital channel filter bandwidth.
		–88		dBm	250kbps data rate (2-FSK), 1% packet error rate, 16 bytes packet length, 460kHz digital channel filter bandwidth.
		–98		dBm	10kbps data rate (2-FSK), 1% packet error rate, 16 bytes packet length, 232kHz digital channel filter bandwidth.
Saturation		–15		dBm	
Digital channel filter bandwidth	58		650	kHz	User programmable. The bandwidth limits are proportional to crystal frequency (given values assume a 26.0MHz crystal).
Adjacent channel rejection		20-25 (TBD)		dB	Desired channel 3dB above the sensitivity limit. Depends on channel spacing and digital channel filter bandwidth.
Alternate channel rejection		25-35 (TBD)		dB	Desired channel 3dB above the sensitivity limit. Depends on channel spacing and digital channel filter bandwidth.
Image channel rejection		30 (TBD)		dB	Desired channel 3dB above the sensitivity limit. Depends on intermediate frequency (IF), channel spacing and digital channel filter bandwidth. Image channel rejection can be limited by adjacent channel rejection or alternate channel rejection when using low IF (<100kHz). Optimum IF depends on data rate and related chip configurations provided by SmartRF® Studio software.
Selectivity at 1MHz offset		–27		dB	Desired channel at –80dBm.
Selectivity at 2MHz offset		–27		dB	Desired channel at –80dBm.
Selectivity at 5MHz offset		–36		dB	Desired channel at –80dBm. Compliant to ETSI EN 300 440 class 2 receiver requirements.
Selectivity at 10MHz offset		–51		dB	Desired channel at –80dBm. Compliant to ETSI EN 300 440 class 2 receiver requirements.
Selectivity at 20MHz offset		–54		dB	Desired channel at –80dBm. Compliant to ETSI EN 300 440 class 2 receiver requirements.
Selectivity at 50MHz offset		–55		dB	Desired channel at –80dBm. Compliant to ETSI EN 300 440 class 2 receiver requirements.
Spurious emissions			–57 –47	dBm dBm	25MHz – 1GHz Above 1GHz

Table 5: RF Receive Section

7 RF Transmit Section

Tc = 25°C, VDD = 3.0V if nothing else stated. Measured on Chipcon's ***CC2500*** EM reference design.

Parameter	Min	Typ	Max	Unit	Condition/Note
Differential load impedance		200		Ω	Optimised for matching to both 50Ω single-ended load and PCB antennas with higher impedance.
Output power, highest setting		1		dBm	Output power is programmable. Delivered to 50Ω single-ended load via Chipcon reference RF matching network.
Output power, lowest setting		–30		dBm	Output power is programmable. Delivered to 50Ω single-ended load via Chipcon reference RF matching network.
Adjacent channel power		–26		dBc	The given values are for 1MHz channel spacing (±1MHz from carrier) and 500kbps MSK.
Alternate channel power		–45		dBc	The given values are for 1MHz channel spacing (±2MHz from carrier) and 500kbps MSK.
Spurious emissions			–36	dBm	25MHz – 1GHz
			–54	dBm	47-74, 87.5-118, 174-230,470-862MHz
			–47	dBm	1800MHz-1900MHz (restricted band in Europe)
			–41	dBm	At 2·RF and 3·RF (restricted bands in USA)
			–30	dBm	Otherwise above 1GHz

Table 6: RF Transmit Parameters

8 Crystal Oscillator

Tc = 25°C @ VDD = 3.0V if nothing else is stated.

Parameter	Min	Typ	Max	Unit	Condition/Note
Crystal frequency	26	26	28	MHz	
Tolerance		±40		ppm	This is the total tolerance including a) initial tolerance, b) ageing and c) temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing / bandwidth.
ESR			100	Ω	
C_0			TBD	pF	
C_L	TBD		TBD	pF	
Start-up time		300		µs	Measured on Chipcon's ***CC2500*** EM reference design.

Table 7: Crystal Oscillator Parameters

9 Low Power RC Oscillator

Typical performance is for Tc = 25°C @ VDD = 3.0V if nothing else is stated.

The values in the table are simulated results and will be updated in later versions of the data sheet.

Parameter	Min	Typ	Max	Unit	Condition/Note
Calibrated frequency	34.6	34.7	37.3	kHz	Calibrated RC Oscillator frequency is XTAL frequency divided by 750
Frequency accuracy after calibration			±0.2	%	
Temperature coefficient		+0.4		% / °C	Frequency drift when temperature changes after calibration
Supply voltage coefficient		+3		% / V	Frequency drift when supply voltage changes after calibration
Initial calibration time		2		ms	When the RC Oscillator is enabled, calibration is continuously done in the background as long as the crystal oscillator is running.
Wake-up period	63e-6		64800	Seconds	Programmable, dependent on XTAL frequency

Table 8: RC Oscillator parameters

10 Frequency Synthesizer Characteristics

Tc = 25°C @ VDD = 3.0V if nothing else is stated. Measured on Chipcon's ***CC2500*** EM reference design.

Parameter	Min	Typ	Max	Unit	Condition/Note
Programmed frequency resolution	397	$F_{XOSC}/2^{16}$	427	Hz	26MHz-28MHz crystal.
Synthesizer frequency tolerance		±40		ppm	Given by crystal used. Required accuracy (including temperature and aging) depends on frequency band and channel bandwidth / spacing.
RF carrier phase noise		–73		dBc/Hz	@ 50kHz offset from carrier
RF carrier phase noise		–73		dBc/Hz	@ 100kHz offset from carrier
RF carrier phase noise		–73		dBc/Hz	@ 200kHz offset from carrier
RF carrier phase noise		–96		dBc/Hz	@ 1MHz offset from carrier
RF carrier phase noise		–106		dBc/Hz	@ 2MHz offset from carrier
RF carrier phase noise		–112		dBc/Hz	@ 5MHz offset from carrier
RF carrier phase noise		–113		dBc/Hz	@ 10MHz offset from carrier
PLL turn-on / hop time			80	µs	Time from leaving the IDLE state until arriving in the RX, FSTXON or TX state, when not performing calibration. Crystal oscillator running.
PLL RX/TX and TX/RX settling time			10	µs	Settling time for the 1xIF frequency step from RX to TX, and vice versa.
PLL calibration time		18739		XOSC cycles	Calibration can be initiated manually, or automatically before entering or after leaving RX/TX.
	0.67	0.72	0.72	ms	Min/typ/max time is for 28/26/26MHz crystal frequency.

Table 9: Frequency Synthesizer Parameters

11 Analog temperature sensor

The characteristics of the analog temperature sensor are listed in Table 10 below. Note that it is necessary to write 0xBF to the PTEST register to use the analog temperature sensor in the IDLE state.

The values in the table are simulated results and will be updated in later versions of the data sheet. Minimum / maximum values are valid over entire supply voltage range. Typical values are for 3.0V supply voltage.

Parameter	Min	Typ	Max	Unit	Condition/Note
Output voltage at –40°C	0.638	0.648	0.706	V	
Output voltage at 0°C	0.733	0.743	0.793	V	
Output voltage at +40°C	0.828	0.840	0.891	V	
Output voltage at +80°C	0.924	0.939	0.992	V	
Output voltage at +120°C	1.022	1.039	1.093	V	
Temperature coefficient	2.35	2.45	2.46	mV/°C	Fitted from –20°C to +80°C
Absolute error in calculated temperature	–14	–8	+14	°C	From –20°C to +80°C when assuming best fit for absolute accuracy: 0.763V at 0°C and 2.44mV / °C
Error in calculated temperature, calibrated	–2		+2	°C	From –20°C to +80°C when using 2.44mV / °C, after 1-point calibration at room temperature
Settling time after enabling		TBD		µs	
Current consumption increase when enabled		0.3		mA	

Table 10: Analog Temperature Sensor Parameters

12 DC Characteristics

The DC Characteristics of *CC2500* are listed in Table 11 below.

Tc = 25°C if nothing else stated.

Digital Inputs/Outputs	Min	Max	Unit	Condition
Logic "0" input voltage	0	0.7	V	
Logic "1" input voltage	VDD-0.7	VDD	V	
Logic "0" output voltage	0	0.5	V	For up to 4mA output current
Logic "1" output voltage	VDD-0.3	VDD	V	For up to 4mA output current
Logic "0" input current	N/A	–1	µA	Input equals 0V
Logic "1" input current	N/A	1	µA	Input equals VDD

Table 11: DC Characteristics

13 Power On Reset

When the power supply complies with the requirements in Table 12 below, proper Power-On-Reset functionality is guaranteed. Otherwise, the chip should be assumed to have unknown state until transmitting an SRES strobe over the SPI interface. It is recommended to transmit an SRES strobe after turning power on in any case. See section 28.1 on page 30 for a description of the recommended start up sequence after turning power on.

Parameter	Min	Typ	Max	Unit	Condition/Note
Power-up ramp-up time.			5	ms	From 0V until reaching 1.8V
Power off time	1			ms	Minimum time between power off and power-on.

Table 12: Power-on Reset Requirements

14 Pin Configuration

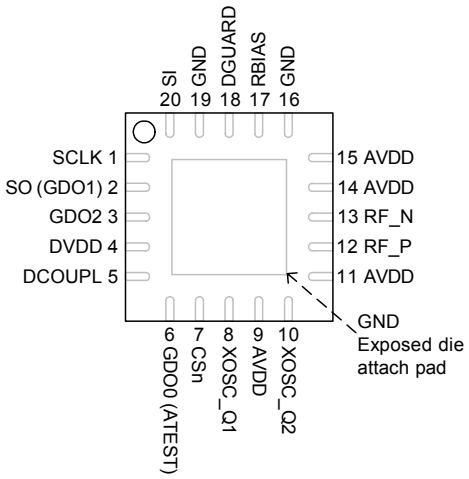

Figure 1: Pinout top view

Note: The exposed die attach pad **must** be connected to a solid ground plane as this is the main ground connection for the chip.

Pin #	Pin name	Pin type	Description
1	SCLK	Digital Input	Serial configuration interface, clock input
2	SO (GDO1)	Digital Output	Serial configuration interface, data output. Optional general output pin when CSn is high
3	GDO2	Digital Output	Digital output pin for general use: • Test signals • FIFO status signals • Clear Channel Indicator • Clock output, down-divided from XOSC • Serial output RX data
4	DVDD	Power (Digital)	1.8V-3.6V digital power supply for digital I/O's and for the digital core voltage regulator
5	DCOUPL	Power (Digital)	1.6V-2.0V digital power supply output for decoupling. NOTE: This pin is intended for use with the ***CC2500*** only. It cannot be used to provide supply voltage to other devices.
6	GDO0 (ATEST)	Digital I/O	Digital output pin for general use: • Test signals • FIFO status signals • Clear Channel Indicator • Clock output, down-divided from XOSC • Serial output RX data • Serial input TX data Also used as analog test I/O for prototype/production testing
7	CSn	Digital Input	Serial configuration interface, chip select
8	XOSC_Q1	Analog I/O	Crystal oscillator pin 1, or external clock input
9	AVDD	Power (Analog)	1.8V-3.6V analog power supply connection
10	XOSC_Q2	Analog I/O	Crystal oscillator pin 2
11	AVDD	Power (Analog)	1.8V-3.6V analog power supply connection
12	RF_P	RF I/O	Positive RF input signal to LNA in receive mode Positive RF output signal from PA in transmit mode
13	RF_N	RF I/O	Negative RF input signal to LNA in receive mode Negative RF output signal from PA in transmit mode
14	AVDD	Power (Analog)	1.8V-3.6V analog power supply connection
15	AVDD	Power (Analog)	1.8V-3.6V analog power supply connection
16	GND	Ground (Analog)	Analog ground connection
17	RBIAS	Analog I/O	External bias resistor for reference current
18	DGUARD	Power (Digital)	Power supply connection for digital noise isolation
19	GND	Ground (Digital)	Ground connection for digital noise isolation
20	SI	Digital Input	Serial configuration interface, data input

Table 13: Pinout overview

15 Circuit Description

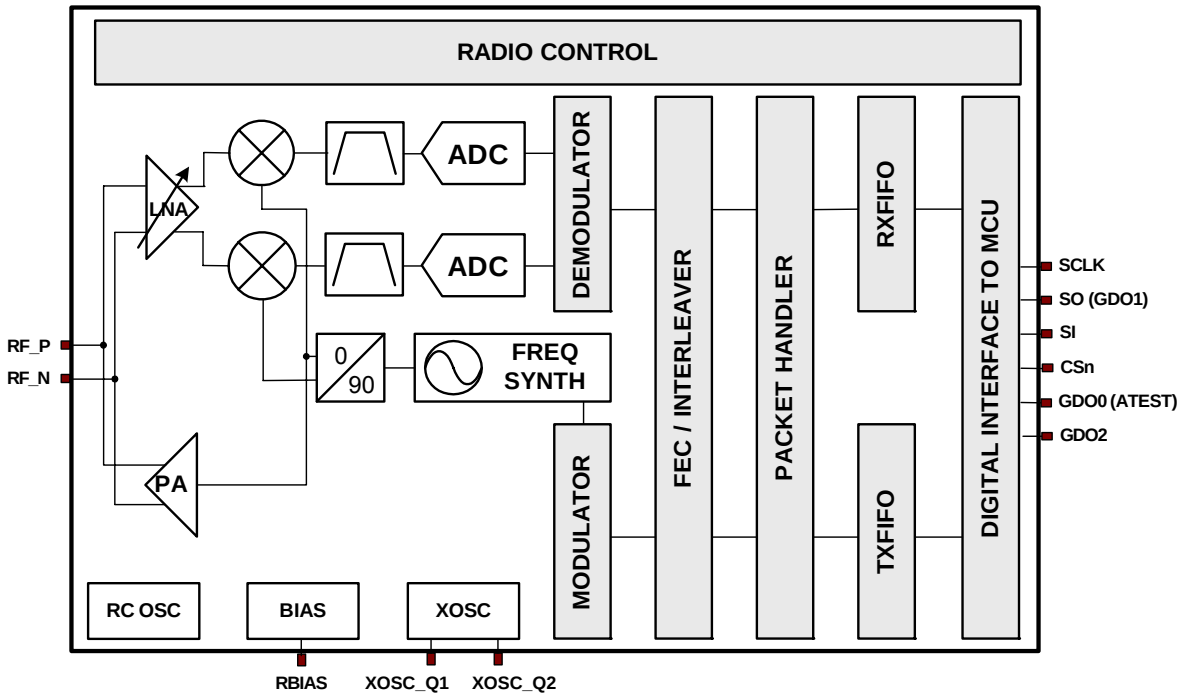

Figure 2: *CC2500* Simplified Block Diagram

A simplified block diagram of ***CC2500*** is shown in Figure 2.

CC2500 features a low-IF receiver. The received RF signal is amplified by the low-noise amplifier (LNA) and down-converted in quadrature (I and Q) to the intermediate frequency (IF). At IF, the I/Q signals are digitised by the ADCs. Automatic gain control (AGC), fine channel filtering, demodulation bit/packet synchronization is performed digitally.

The transmitter part of ***CC2500*** is based on direct synthesis of the RF frequency. The frequency synthesizer includes a completely on-chip LC VCO and a 90 degrees phase shifter for generating the I and Q LO signals to the down-conversion mixers in receive mode.

A crystal is to be connected to XOSC_Q1 and XOSC_Q2. The crystal oscillator generates the reference frequency for the synthesizer, as well as clocks for the ADC and the digital part.

A 4-wire SPI serial interface is used for configuration and data buffer access.

The digital baseband includes support for channel configuration, packet handling and data buffering.

16 Application Circuit

Only a few external components are required for using the ***CC2500***. The recommended application circuit is shown in Figure 3. The external components are described in Table 14, and typical values are given in Table 15. Note that the PCB antenna alternative indicated in Figure 3 is preliminary and subject to changes. Performance for the PCB antenna alternative will be included in future revisions of this data sheet.

Bias resistor

The bias resistor R171 is used to set an accurate bias current.

Balun and RF matching

C122, C132, L121 and L131 form a balun that converts the differential RF port on ***CC2500*** to a single-ended RF signal (C121 and C131 are also needed for DC blocking). Together with an appropriate LC network, the balun components also transform the impedance to match a 50Ω antenna (or cable). Component

values for the RF balun and LC network are easily found using the SmartRF® Studio software. Suggested values are listed in Table 15.

Crystal

The crystal oscillator uses an external crystal with two loading capacitors (C81 and C101). See section 34 on page 36 for details.

Power supply decoupling

The power supply must be properly decoupled close to the supply pins. Note that decoupling capacitors are not shown in the application circuit. The placement and the size of the decoupling capacitors are very important to achieve the optimum performance. Chipcon provides a reference design that should be followed closely.

Component	Description
C51	100nF decoupling capacitor for on-chip voltage regulator to digital part
C81/C101	Crystal loading capacitors, see section 34 on page 36 for details
C121/C131	RF balun DC blocking capacitors
C122/C132	RF balun/matching capacitors
C123/C124	RF LC filter/matching capacitors
L121/L131	RF balun/matching inductors (inexpensive multi-layer type)
L122	RF LC filter inductor (inexpensive multi-layer type)
R171	56kΩ resistor for internal bias current reference
XTAL	26MHz-28MHz crystal, see section 34 on page 36 for details

Table 14: Overview of external components (excluding supply decoupling capacitors)

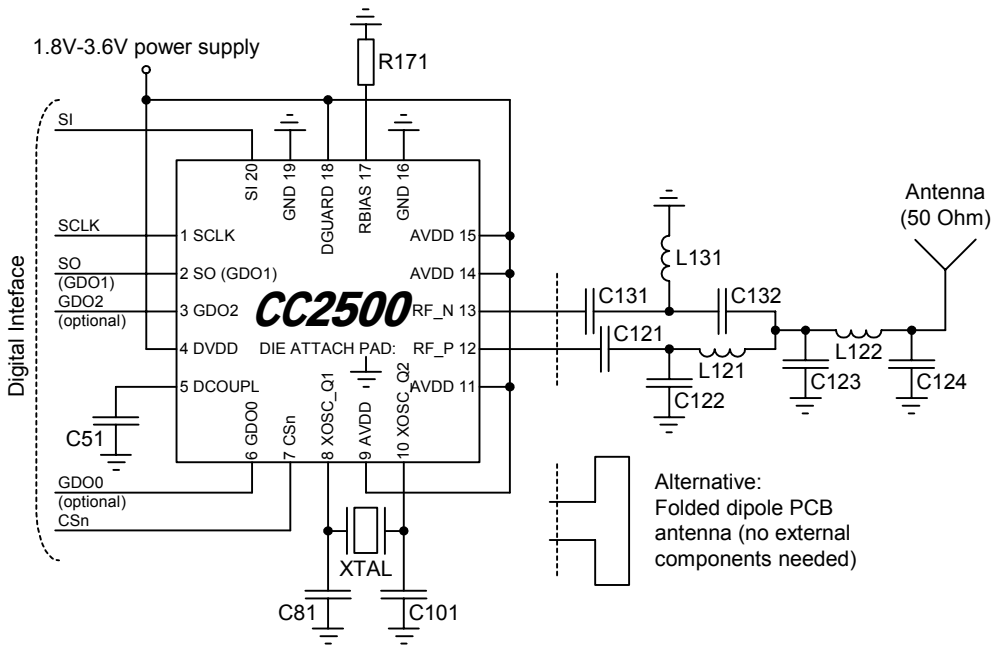

Figure 3: Typical application and evaluation circuit (power supply decoupling not shown)

Component	Value
C51	100nF±10%, 0402 X5R
C81	27pF±5%, 0402 NP0
C101	27pF±5%, 0402 NP0
C121	100pF±5%, 0402 NP0
C122	1.0pF±0.25pF, 0402 NP0
C123	1.8pF±0.25pF, 0402 NP0
C124	1.5pF±0.25pF, 0402 NP0
C131	100pF±5%, 0402 NP0
C132	1.0pF±0.25pF, 0402 NP0
L121	1.2nH±0.3nH, 0402 monolithic
L122	1.2nH±0.3nH, 0402 monolithic
L131	1.2nH±0.3nH, 0402 monolithic
R171	56kΩ±1%, 0402
XTAL	26.0MHz surface mount crystal

Table 15: Bill Of Materials for the application circuit (subject to changes)

17 Configuration Overview

CC2500 can be configured to achieve optimum performance for many different applications. Configuration is done using the SPI interface. The following key parameters can be programmed:

- Power-down / power up mode
- Crystal oscillator power-up / power – down
- Receive / transmit mode
- RF channel selection
- Data rate
- Modulation format
- RX channel filter bandwidth
- RF output power
- Data buffering with separate 64-byte receive and transmit FIFOs
- Packet radio hardware support
- Forward Error Correction with interleaving
- Data Whitening
- Wake On Radio (WOR)

Details of each configuration register can be found in section 38, starting on page 39.

Figure 4 shows a simplified state diagram that explains the main ***CC2500*** states, together with typical usage and current consumption. For detailed information on controlling the ***CC2500*** state machine, and a complete state diagram, see section 28, starting on page 29.

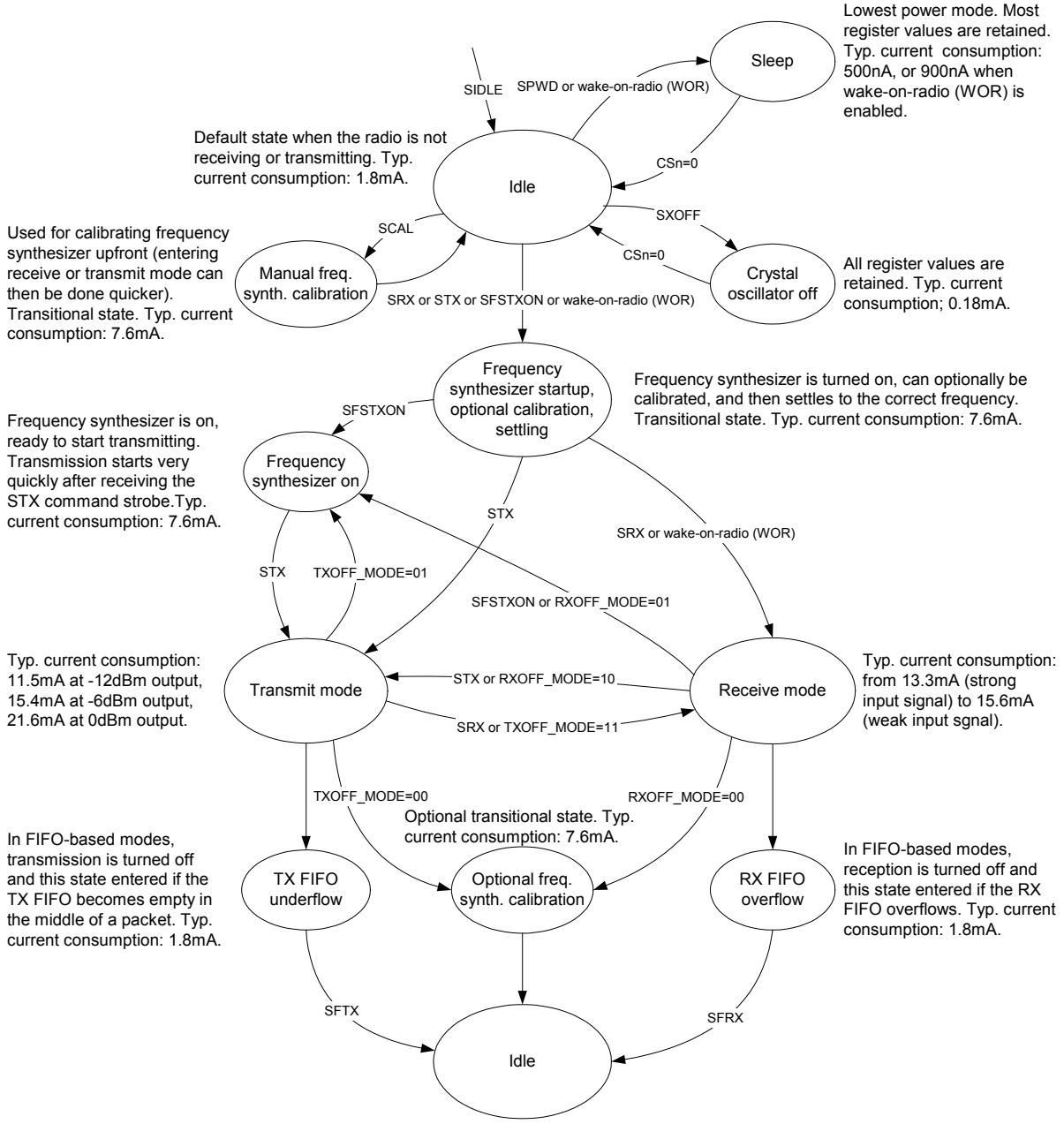

Figure 4: Simplified state diagram, with typical usage and current consumption

18 Configuration Software

CC2500 can be configured using the SmartRF® Studio software, available for download from http://www.chipcon.com. The SmartRF® Studio software is highly recommended for obtaining optimum register settings, and for evaluating performance and functionality. A screenshot of the SmartRF® Studio user interface for ***CC2500*** is shown in Figure 5.

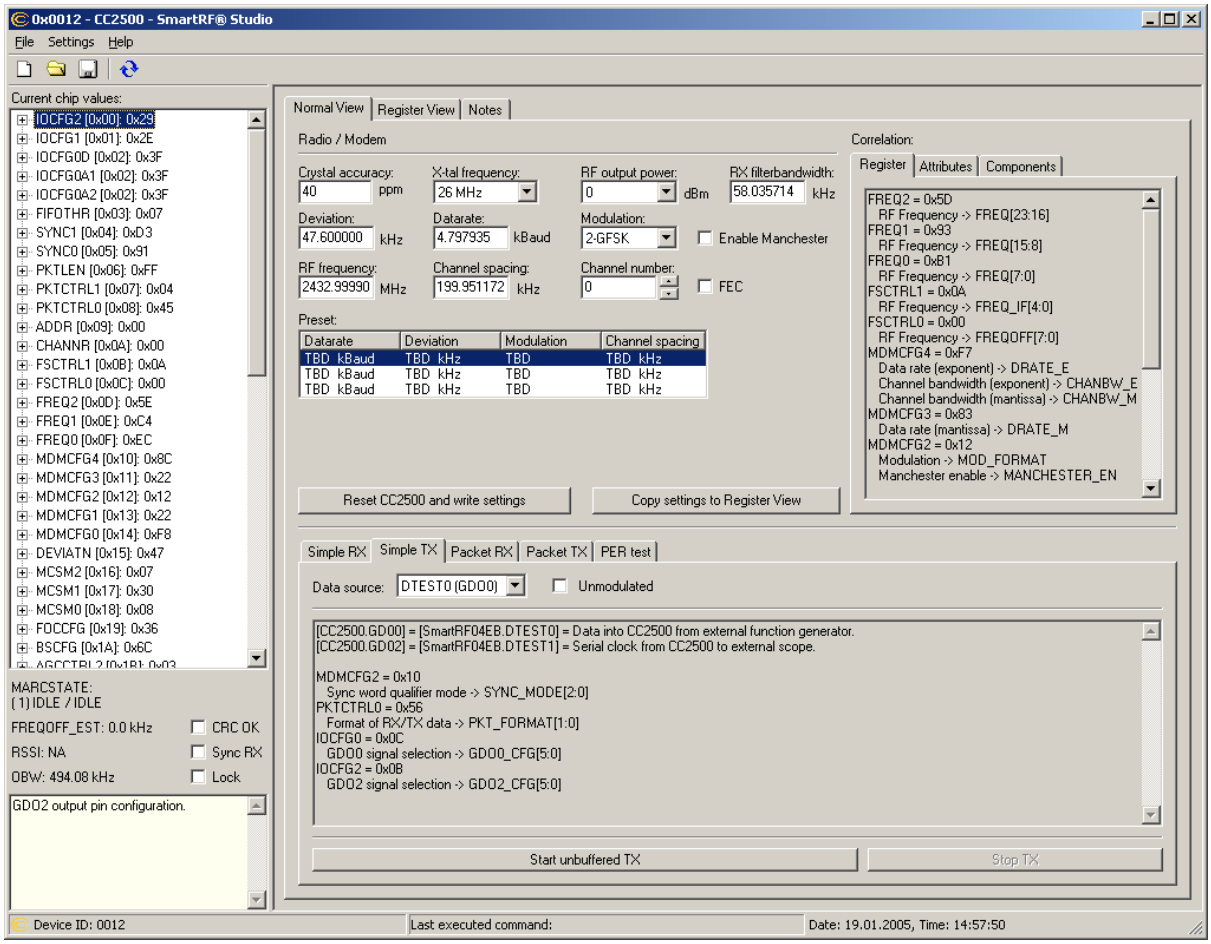

Figure 5: SmartRF® Studio user interface

19 4-wire Serial Configuration and Data Interface

CC2500 is configured via a simple 4-wire SPI-compatible interface (SI, SO, SCLK and CSn) where ***CC2500*** is the slave. This interface is also used to read and write buffered data. All address and data transfer on the SPI interface is done most significant bit first.

All transactions on the SPI interface start with a header byte containing a read/write bit, a burst access bit and a 6-bit address.

During address and data transfer, the CSn pin (Chip Select, active low) must be kept low. If CSn goes high during the access, the transfer will be cancelled.

When CSn goes low, the MCU must wait until the SO pin from ***CC2500*** goes low before starting to transfer the header byte. This indicates that the voltage regulator has stabilized and the crystal is running. Unless the chip was in the SLEEP or XOFF states, the SO pin will always go low immediately after taking CSn low.

19.1 Chip Status Byte

When the header byte is sent on the SPI interface, the chip status byte is sent by the ***CC2500*** on the SO pin. The status byte contains key status signals, useful for the MCU. The first bit, s7, is the CHIP_RDYn signal; this signal must go low before the first positive edge of SCLK. The CHIP_RDYn signal indicates that the crystal is running and the regulated digital supply voltage is stable.

Bit 6, 5 and 4 comprises the STATE value. This value reflects the state of the chip. When idle the XOSC and power to the digital core is on, but all other modules are in power down. The frequency and channel configuration should only be updated when the chip is in this state.

The RX state will be active when the chip is in receive mode. Likewise, TX is active when the chip is transmitting.

The last four bits (3:0) in the status byte contains FIFO_BYTES_AVAILABLE. For read operations, the FIFO_BYTES_AVAILABLE field contains the number of bytes available for reading from the RX FIFO. For write operations, the FIFO_BYTES_AVAILABLE field contains the number of bytes free for writing into the TX FIFO. When FIFO_BYTES_AVAILABLE=15, 15 or more bytes are available/free.

19.2 Registers Access

The configuration registers on the ***CC2500*** are located on SPI addresses from 0x00 to 0x2F. Table 26 on page 41 lists all configuration registers. The detailed description of each register is found in Section 38.1, starting on page 44. All configuration registers can be both written and read. The read/write bit controls if the register should be written or read. When writing to registers, the status byte is sent on the SO pin each time a data byte to be written is transmitted on the SI pin.

Registers with consecutive addresses can be accessed in an efficient way by setting the burst bit in the address header. The address sets the start address in an internal address counter. This counter is incremented by one each new byte (every 8 clock pulses). The burst access is either a read or a write access and must be terminated by setting CSn high.

For register addresses in the range 0x30-0x3D, the “burst” bit is used to select between status registers and command strobes (see below). The status registers can only be read. Burst read is not available for status registers, so they must be read one at a time.

19.3 Command Strobes

Command Strobes may be viewed as single byte instructions to ***CC2500***. By addressing a Command Strobe register, internal sequences will be started. These commands are used to disable the crystal oscillator, enable receive mode, enable wake-on-radio etc. The 14 command strobes are listed in Table 25 on page 40.

The command strobe registers are accessed in the same way as for a register write operation, but no data is transferred. That is, only the R/W bit (set to 0), burst access (set to 0) and the six address bits (in the range 0x30 through 0x3D) are written. A command strobe may be followed by any other SPI access without pulling CSn high. The command strobes are executed immediately, with the exception of the SPWD and the SXOFF strobes that are executed when CSn goes high.

19.4 FIFO Access

The 64-byte TX FIFO and the 64-byte RX FIFO are accessed through the 0x3F address. When the read/write bit is zero, the TX FIFO is accessed, and the RX FIFO is accessed when the read/write bit is one.

The TX FIFO is write-only, while the RX FIFO is read-only.

The burst bit is used to determine if FIFO access is single byte or a burst access. The single byte access method expects address with burst bit set to zero and one data byte. After the data byte a new address is expected; hence, CSn can remain low. The burst access method expects one address byte and then consecutive data bytes until terminating the access by setting CSn high.

The following header bytes access the FIFOs:

- 0x3F: Single byte access to TX FIFO
- 0x7F: Burst access to TX FIFO
- 0xBF: Single byte access to RX FIFO
- 0xFF: Burst access to RX FIFO

When writing to the TX FIFO, the status byte (see Section 19.1) is output for each new data byte on SO, as shown in Figure 6. This status byte can be used to detect TX FIFO underflow while writing data to the TX FIFO. Note that the status byte contains the number of bytes free *before* writing the byte in progress to the TX FIFO. When the last byte that fits in the TX FIFO is transmitted to the SI pin, the status byte received concurrently on the SO pin will indicate that one byte is free in the TX FIFO.

The transmit FIFO may be flushed by issuing a SFTX command strobe. Similarly, a SFRX command strobe will flush the receive FIFO. Both FIFOs are cleared when going to the SLEEP state.

19.5 PATABLE Access

The 0x3E address is used to access the PATABLE, which is used for selecting PA power control settings. The SPI expects up to eight data bytes after receiving the address. By programming the PATABLE, controlled PA power ramp-up and ramp-down can be achieved, as well as ASK modulation shaping for reduced bandwidth. See section 33 on page 35 for output power programming details.

The PATABLE is an 8-byte table that defines the PA control settings to use for each of the eight PA power values (selected by the 3-bit value FREND0.PA_POWER). The table is written and read from the lowest setting (0) to the highest (7), one byte at a time. An index counter is used to control the access to the table. This counter is incremented each time a byte is read or written to the table, and set to the lowest index when CSn is high. When the highest value is reached the counter restarts at zero.

The access to the PATABLE is either single byte or burst access depending on the burst bit. When using burst access the index counter will count up; when reaching 7 the counter will restart at 0. The read/write bit controls whether the access is a write access (R/W=0) or a read access (R/W=1).

If one byte is written to the PATABLE and this value is to be read out then CSn must be set high before the read access in order to set the index counter back to zero.

Note that the content of the PATABLE is lost when entering the SLEEP state, except for the first byte (index 0).

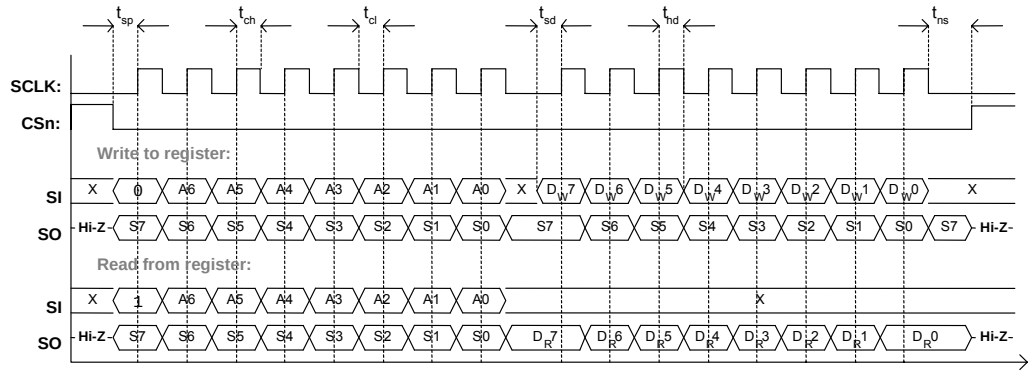

Figure 6: Configuration registers write and read operations

Parameter	Description	Min	Max
F_{SCLK}	SCLK frequency	0	10MHz
$t_{sp,pd}$	CSn low to positive edge on SCLK, in power-down mode	TBDμs	-
t_{sp}	CSn low to positive edge on SCLK, in active mode	TBDns	-
t_{ch}	Clock high	50ns	-
t_{cl}	Clock low	50ns	-
t_{rise}	Clock rise time	-	TBDns
t_{fall}	Clock rise time	-	TBDns
t_{sd}	Setup data to positive edge on SCLK	TBDns	-
t_{hd}	Hold data after positive edge on SCLK	TBDns	-
t_{ns}	Negative edge on SCLK to CSn high.	TBDns	-

Table 16: SPI interface timing requirements

Bits	Name	Description
7	CHIP_RDYn	Stays high until power and crystal have stabilized. Should always be low when using the SPI interface.
6:4	STATE[2:0]	Indicates the current main state machine mode

Value	State	Description
000	Idle	IDLE state (Also reported for some transitional states instead of SETTLING or CALIBRATE, due to a small error)
001	RX	Receive mode
010	TX	Transmit mode
011	FSTXON	Fast TX ready
100	CALIBRATE	Frequency synthesizer calibration is running
101	SETTLING	PLL is settling
110	RXFIFO_OVERFLOW	RX FIFO has overflowed. Read out any useful data, then flush the FIFO with SFRX
111	TXFIFO_UNDERFLOW	TX FIFO has underflowed. Acknowledge with SFTX

3:0	FIFO_BYTES_AVAILABLE[3:0]	The number of bytes available in the RX FIFO or free bytes in the TX FIFO (depends on the read/write-bit). If FIFO_BYTES_AVAILABLE=15, it indicates that 15 or more bytes are available/free.

Table 17: Status byte summary

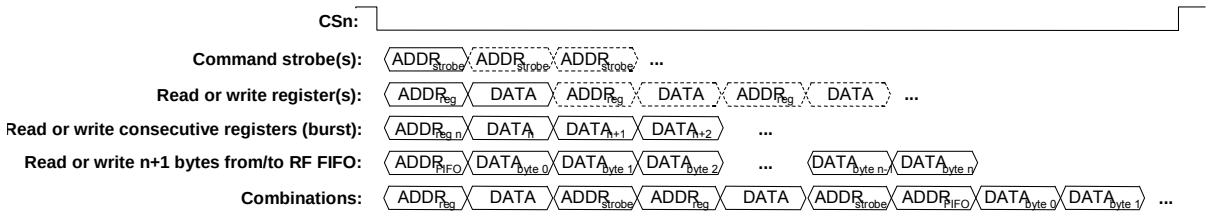

Figure 7: Register access types

20 Microcontroller Interface and Pin Configuration

In a typical system, ***CC2500*** will interface to a microcontroller. This microcontroller must be able to:

- Program ***CC2500*** into different modes,
- Read and write buffered data
- Read back status information via the 4-wire SPI-bus configuration interface (SI, SO, SCLK and CSn).

20.1 Configuration Interface

The microcontroller uses four I/O pins for the SPI configuration interface (SI, SO, SCLK and CSn). The SPI is described in Section 0 on page 16.

20.2 General Control and Status Pins

The ***CC2500*** has two dedicated configurable pins and one shared pin that can output internal status information useful for control software. These pins can be used to generate

interrupts on the MCU. See Section 36 page 37 for more details of the signals that can be programmed. The dedicated pins are called GDO0 and GDO2. The shared pin is the SO pin in the SPI interface. The default setting for GDO1/SO is 3-state output. By selecting any other of the programming options the GDO1/SO pin will become a generic pin. When CSn is low, the pin will always function as a normal SO pin.

In the synchronous and asynchronous serial modes, the GDO0 pin is used as a serial TX data input pin while in transmit mode.

The GDO0 pin can also be used for an on-chip analog temperature sensor. By measuring the voltage on the GDO0 pin with an external ADC, the temperature can be calculated. Specifications for the temperature sensor are found in section 11 on page 10.

The temperature sensor output is usually only available when the frequency synthesizer is enabled (e.g. the MANCAL, FSTXON, RX and TX states). It is necessary to write 0xBF to the PTEST register to use the analog temperature sensor in the IDLE state. Before leaving the IDLE state, the PTEST register should be restored to its default value (0x7F).

20.3 Optional radio control feature

The ***CC2500*** has an optional way of controlling the radio, by reusing SI, SCLK and CSn from the SPI interface. This feature allows for a simple three-pin control of the major states of the radio: SLEEP, IDLE, RX and TX.

This optional functionality is enabled with the MCSM0.PIN_CTRL_EN configuration bit.

State changes are commanded as follows when CSn is high the SI and SCLK is set to the desired state according to Table 18. When CSn goes low the state of SI and SCLK is latched and a command strobe is generated internally according to the pin configuration. It is only possible to change state with this functionality. That means that for instance RX will not be restarted if SI and SCLK are set to RX and CSn toggles. When CSn is low the SI and SCLK has normal SPI functionality.

CSn	SCLK	SI	Function
1	X	X	Chip unaffected by SCLK/SI
↓	0	0	Generates SPWD strobe
↓	0	1	Generates STX strobe
↓	1	0	Generates SIDLE strobe
↓	1	1	Generates SRX strobe
0	SPI mode	SPI mode	SPI mode (wakes up into IDLE if in SLEEP/XOFF)

Table 18: Optional pin control coding

All pin control command strobes are executed immediately, except the SPWD strobe, which is delayed until CSn goes high.

21 Data Rate Programming

The data rate used when transmitting, or the data rate expected in receive is programmed by the MDMCFG3.DRATE_M and the MDMCFG4.DRATE_E configuration registers. The data rate is given by the formula below. As the formula shows, the programmed data rate depends on the crystal frequency.

$$R_{DATA} = \frac{(256 + DRATE\_M) \cdot 2^{DRATE\_E}}{2^{28}} \cdot f_{XOSC}$$

The following approach can be used to find suitable values for a given data rate:

$$DRATE\_E = \left\lfloor \log_2 \left(\frac{R_{DATA} \cdot 2^{20}}{f_{XOSC}} \right) \right\rfloor$$

$$DRATE\_M = \frac{R_{DATA} \cdot 2^{28}}{f_{XOSC} \cdot 2^{DRATE\_E}} - 256$$

If DRATE_M is rounded to the nearest integer and becomes 256, increment DRATE_E and use DRATE_M=0.

22 Receiver Channel Filter Bandwidth

In order to meet different channel width requirements, the receiver channel filter is programmable. The MDMCFG4.CHANBW_E and MDMCFG4.CHANBW_M configuration registers

control the receiver channel filter bandwidth, which scales with the crystal oscillator frequency. The following formula gives the relation between the register settings and the channel filter bandwidth:

$$BW_{channel} = \frac{f_{XOSC}}{8 \cdot (4 + CHANBW\_M) \cdot 2^{CHANBW\_E}}$$

The ***CC2500*** supports channel filter bandwidths between 54-63kHz and 600-700kHz[1]. Above 300kHz bandwidth, however, the sensitivity and blocking performance may be somewhat degraded.

[1] The combination of CHANBW_E=0 and CHANBW_M=0 is not supported. Exact limits depend on crystal frequency.

For best performance, the channel filter bandwidth should be selected so that the signal bandwidth occupies at most 80% of the channel filter bandwidth. The channel centre tolerance due to crystal accuracy should also be subtracted from the signal bandwidth. The following example illustrates this:

With the channel filter bandwidth set to 600kHz, the signal should stay within 80% of 600kHz, which is 480kHz. Assuming 2.44GHz frequency and ±20ppm frequency uncertainty for both the transmitting device and the receiving device, the total frequency uncertainty is ±40ppm of 2.44GHz, which is ±98kHz. If the whole transmitted signal bandwidth is to be received within 480kHz, the transmitted signal bandwidth should be maximum 480kHz–2·98kHz, which is 284kHz.

23 Demodulator, Symbol Synchronizer and Data Decision

CC2500 contains an advanced and highly configurable demodulator. Channel filtering and frequency offset compensation is performed digitally. To generate the RSSI level (see section 26.2 for more information) the signal level in the channel is estimated. Data filtering is also included for enhanced performance.

23.1 Frequency Offset Compensation

When using FSK or MSK modulation, the demodulator will compensate for the offset between the transmitter and receiver frequency, within certain limits, by estimating the centre of the received data. This value is available in the FREQEST status register.

By issuing the SAFC command strobe, the measured offset, FREQEST.FREQOFF_EST, can automatically be used to adjust the frequency offset programming in the frequency synthesizer. This will add the current RX frequency offset estimate to the value in FSCTRL0.FREQOFF, which adjust the synthesizer frequency. Thus, the frequency offset will be compensated in both RX and TX when the SAFC command strobe is used.

To avoid compensating for frequency offsets measured without a valid signal in the RF channel, FREQEST.FREQOFF_EST is copied to an internal register when issuing the SAFC strobe in RX, and when a synch word is detected. If SAFC was issued in RX, this internal value is added to FSCTRL0.FREQOFF after exiting RX. Issuing SAFC when not in RX will immediately add the internal register value to FSCTRL0.FREQOFF. Thus, the SAFC strobe should be issued when currently receiving a packet, or outside the RX state.

Note that frequency offset compensation is not supported for ASK or OOK modulation.

23.2 Bit Synchronization

The bit synchronization algorithm extracts the clock from the incoming symbols. The algorithm requires that the expected data rate is programmed as described in Section 21 on page 21. Re-synchronization is performed continuously to adjust for error in the incoming symbol rate.

23.3 Byte synchronization

Byte synchronization is achieved by a continuous sync word search. The sync word is a 16 or 32 bit configurable field that is automatically inserted at the start of the packet by the modulator in transmit mode. The demodulator uses this field to find the byte boundaries in the stream of bits. The sync word will also function as a system identifier, since only packets with the correct predefined sync word will be received. The sync word detector correlates against the user-configured 16-bit sync word. The correlation threshold can be set to 15/16 bits match or 16/16 bits

match. The sync word can be further qualified using the preamble quality indicator mechanism described below and/or a carrier sense condition. The sync word is programmed with SYNC1 and SYNC0.

In order to make false detections of sync words less likely, a mechanism called preamble quality indication (PQI) can be used to qualify the sync word. A threshold value for the preamble quality must be exceeded in order for a detected sync word to be accepted. See section 26.1 on page 26 for more details.

24 Packet Handling Hardware Support

The ***CC2500*** has built-in hardware support for packet oriented radio protocols.

In transmit mode, the packet handler will add the following elements to the packet stored in the TX FIFO:

- A programmable number of preamble bytes.
- A two byte Synchronization Word. Can be duplicated to give a 4-byte sync word.
- Optionally whiten the data with a PN9 sequence.
- Optionally Interleave and Forward Error Code the data.
- Optionally compute and add a CRC checksum over the data field.

In receive mode, the packet handling support will de-construct the data packet:

- Preamble detection.
- Sync word detection.
- Optional one byte address check.
- Optionally compute and check CRC.
- Optionally append two status bytes with RSSI value, Link Quality Indication and CRC status.

The recommended setting is 4-byte preamble and 2-byte sync word.
Note that register fields that control the packet handling features should only be altered when ***CC2500*** is in the IDLE state.

24.1 Data whitening

From a radio perspective, the ideal over the air data are random and DC free. This results in the smoothest power distribution over the occupied bandwidth. This also gives the regulation loops in the receiver uniform operation conditions (no data dependencies).

Real world data often contain long sequences of zeros and ones. Performance can then be improved by whitening the data before transmitting, and de-whitening in the receiver. With ***CC2500***, this can be done automatically by setting PKTCTRL0.WHITE_DATA=1. All data, except the preamble and the sync word, are then XOR-ed with a 9-bit pseudo-random (PN9) sequence before being transmitted. At the receiver end, the data are XOR-ed with the same pseudo-random sequence. This way, the whitening is reversed, and the original data appear in the receiver.

Setting PKTCTRL0.WHITE_DATA=1 is recommended for all uses, except when over-the-air compatibility with other systems is needed.

24.2 Packet format

The format of the data packet can be configured and consists of the following items:

- Preamble
- Synchronization word
- Length byte or constant programmable packet length
- Optional Address byte
- Payload
- Optional 2 byte CRC

The preamble pattern is an alternating sequence of ones and zeros (01010101…). The minimum length of the preamble is programmable. When enabling TX, the modulator will start transmitting the preamble. When the programmed number of preamble bytes has been transmitted, the modulator will send the sync word and then data from the TX FIFO if data is available. If the TX FIFO is empty, the modulator will continue to send preamble bytes until the first byte is written to the TX FIFO. The modulator will then send the sync word and then the data bytes.
The number of preamble bytes is programmed with the MDMCFG1.NUM_PREAMBLE value.

The synchronization word is a two-byte value set in the SYNC1 and SYNC0 registers. The sync word provides byte synchronization of the incoming packet. A one-byte synch word can

be emulated by setting the SYNC1 value to the preamble pattern. It is also possible to emulate a 32 bit sync word by using MDMCFG2.SYNC_MODE=3 or 7. The sync word will then be repeated twice.

CC2500 supports both constant packet length protocols and variable length protocols. The maximum packet length is 255 bytes. Constant packet length mode is selected by setting PKTCTRL0.LENGTH_CONFIG=0. The desired packet length is set by the PKTLEN register. The packet length is defined as the payload data, excluding the length byte and the optional automatic CRC. In variable length mode, the PKTLEN register is used to set the maximum packet length allowed in RX. Any packet received with a length byte with a value greater than PKTLEN will be discarded.

Note that the minimum packet length supported (excluding the optional length byte and CRC) is one byte of payload data.

With PKTCTRL0.LENGTH_CONFIG=2, the packet length is set to infinite and transmission and reception will continue until turned off manually. The infinite mode can be turned off while a packet is being transmitted or received. As described in the next section, this can be used to support packet formats with different length configuration than natively supported by ***CC2500***.

24.2.1 Arbitrary length field configuration

The fixed length field can be reprogrammed during receive and transmit. This opens the possibility to have a different length field configuration than supported for variable length packets. At the start of reception, the packet length is set to a large value. The MCU reads out enough bytes to interpret the length field in the packet. Then the PKTLEN value is set according to this value. The end of packet will occur when the byte counter in the packet handler is equal to the PKTLEN register. Thus, the MCU must be able to program the correct length, before the internal counter reaches the packet length.

By utilizing the infinite packet length option, arbitrary packet length is available. At the start of the packet, the infinite mode must be active. When less than 256 bytes remains of the packet, the MCU sets the PKTLEN register to mod(length, 256), disables infinite packet length and activates fixed length packets. When the internal byte counter reaches the PKTLEN value, the transmission or reception ends. Automatic CRC appending/checking can be used (by setting PKTCTRL0.CRC_EN to 1).

When for example a 454-byte packet is to be transmitted, the MCU does the following:

- Set PKTCTRL0.LENGTH_CONFIG=2 (10).
- Pre-program the PKTLEN register to mod(454,256)=198.
- Transmit at least 198 bytes, for example by filling the 64-byte TX FIFO four times (256 bytes transmitted).
- Set PKTCTRL0.LENGTH_CONFIG=0 (00).
- The transmission ends when the packet counter reaches 198. A total of 256+198=454 bytes are transmitted.

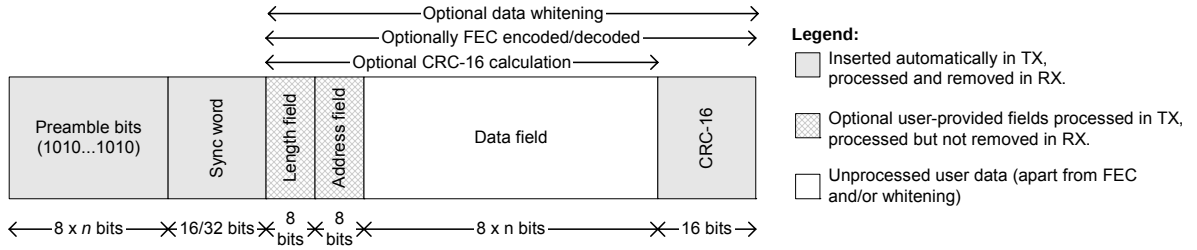

Figure 8: Packet Format

24.3 Packet filtering in Receive Mode

CC2500 supports two different packet-filtering criteria: address filtering and maximum length filtering.

Setting PKTCTRL1.ADR_CHK to any other value than zero enables the packet address filter. The packet handler engine will compare the destination address byte in the packet with the programmed node address in the ADDR

register and the 0x00 broadcast address when PKTCTRL1.ADR_CHK=10 or both 0x00 and 0xFF broadcast addresses when PKTCTRL1.ADR_CHK=11. If the received address matches a valid address, the packet is received and written into the RX FIFO. If the address match fails, the packet is discarded.

In the variable packet length mode the PKTLEN.PACKET_LENGTH register value is used to set the maximum allowed packet length. If the received length byte has a larger value than this, the packet is discarded.

In both cases, receive mode is restarted after discarding the current packet (regardless of the MCSM1.RXOFF_MODE setting).

24.4 Packet Handling in Transmit Mode

The payload that is to be transmitted must be written into the TX FIFO. The first byte written must be the length byte when variable packet length is enabled. The length byte has a value equal to the payload of the packet (including the optional address byte). If fixed packet length is enabled, then the first byte written to the TX FIFO is interpreted as the destination address, if this feature is enabled in the device that receives the packet.

The modulator will first send the programmed number of preamble bytes. If data is available in the TX FIFO, the modulator will send the two-byte (optionally 4-byte) sync word and then the payload in the TX FIFO. If CRC is enabled, the checksum is calculated over all the data pulled from the TX FIFO and the result is sent as two extra bytes at the end of the payload data.

If whitening is enabled, the length byte, payload data and the two CRC bytes will be whitened. This is done before the optional FEC/Interleaver stage. Whitening is enabled by setting PKTCTRL0.WHITE_DATA=1.

If FEC/Interleaving is enabled, the length byte, payload data and the two CRC bytes will be scrambled by the interleaver, and FEC encoded before being modulated.

24.5 Packet Handling in Receive Mode

In receive mode, the demodulator and packet handler will search for a valid preamble and the sync word. When found, the demodulator has obtained both bit and byte synchronism and will receive the first payload byte.

If FEC/Interleaving is enabled, the FEC decoder will start to decode the first payload byte. The interleaver will de-scramble the bits before any other processing is done to the data.

If whitening is enabled, the data will be de-whitened at this stage.

When variable packet length is enabled, the first byte is the length byte. The packet handler stores this value as the packet length and receives the number of bytes indicated by the length byte. If fixed packet length is used, the packet handler will accept the programmed number of bytes.

Next, the packet handler optionally checks the address and only continues the reception if the address matches. If automatic CRC check is enabled, the packet handler computes CRC and matches it with the appended CRC checksum.

At the end of the payload, the packet handler will optionally write two extra packet status bytes that contain CRC status, link quality indication and RSSI value.

25 Modulation Formats

CC2500 supports amplitude, frequency and phase shift modulation formats. The desired modulation format is set in the MDMCFG2.MOD_FORMAT register.

Optionally, the data stream can be Manchester coded by the modulator and decoded by the demodulator. This option is enabled by setting MDMCFG2.MANCHESTER_EN=1. Manchester encoding is not supported at the same time as using the FEC/Interleaver option. Manchester coding can be used with the 2-ary modulation formats (2-FSK, ASK/OOK and MSK).

25.1 Frequency Shift Keying

The frequency deviation is programmed with the DEVIATION_M and DEVIATION_E values in the DEVIATN register. The value has an exponent/mantissa form, and the resultant deviation is given by:

$$f_{dev} = \frac{f_{xosc}}{2^{17}} \cdot (8 + DEVIATION\_M) \cdot 2^{DEVIATION\_E}$$

The symbol encoding is shown in Table 19.

Format	Symbol	Coding
2FSK	'0'	– Deviation
	'1'	+ Deviation

Table 19: Symbol encoding for FSK modulation

25.2 Phase Shift Keying

When using MSK[2], the complete transmission (preamble, sync word and payload) will be MSK modulated.

Phase shifts are performed with a constant transition time. This means that the rate of change for the 180-degree transition is twice that of the 90-degree transition.

The fraction of a symbol period used to change the phase can be modified with the DEVIATN.DEVIATION_M setting. This is equivalent to changing the shaping of the symbol.

25.3 Amplitude Modulation

CC2500 supports two different forms of amplitude modulation: On-Off Keying (OOK) and Amplitude Shift Keying (ASK). OOK modulation simply turns on or off the PA to modulate 1 and 0 respectively. When using ASK the modulation depth (the difference between 1 and 0) can be programmed, and the power ramping will be shaped. This will produce a more bandwidth constrained output spectrum.

[2] Identical to offset QPSK with half-sine shaping (data coding may differ)

26 Received Signal Qualifiers and Link Quality Information

CC2500 has several qualifier values that are used to increase the requirements that must be fulfilled before a search for a valid sync word is started.

26.1 Preamble Quality Threshold (PQT)

The Preamble Quality Threshold (PQT) sync-word qualifier adds the requirement that the received sync word must be preceded with a preamble with a quality above the programmed threshold.

Another use of the preamble quality threshold is as a qualifier for the optional RX termination timer. See section 28.7 on page 32 for details.

The preamble quality estimator increases an internal counter by one each time a bit is received that is different from the previous bit, and decreases the counter by 4 each time a bit is received that is the same as the last bit. The counter saturates at 0 and 31. The threshold is configured with the register field PKTCTRL1.PQT. A threshold of 4·PQT for this counter is used to gate sync word detection. By setting the value to zero, the preamble quality qualifier of the synch word is disabled.

A "Preamble Quality reached" flag can also be observed on one of the GDO pins and in the status register bit PKTSTATUS.PQT_REACHED. This flag asserts when the received signal exceeds the PQT.

26.2 RSSI

The RSSI value is an estimate of the signal level in the current channel. This value is based on the current gain setting in the RX chain and the measured signal level in the channel.

In RX mode, the RSSI value can be read continuously from the RSSI status register, until the demodulator detects a sync word (when sync word detection is enabled). At that point, the RSSI readout value is frozen until the next time the chip enters the RX state. The RSSI value is in dB with ½dB resolution.

If PKTCTRL1.APPEND_STATUS is enabled, a snapshot of the RSSI during the first 8 bytes of the packet is automatically added to the end of each received packet.

26.3 Carrier Sense (CS)

The Carrier Sense flag is used as a sync word qualifier and for CCA. The CS flag can be set based on two conditions, which can be individually adjusted:

- CS is asserted when the RSSI is above a programmable absolute threshold, and de-asserted when RSSI is below the same threshold (with hysteresis).
- CS is asserted when the RSSI has increased with a programmable number of dB from one RSSI sample to the next, and de-asserted when RSSI has decreased with the same number of dB. This setting is not dependent on the absolute signal level and is thus useful to detect signals in environments with time varying noise floor.

Carrier Sense (CS) can be used as a sync word qualifier that requires the signal level to be higher than the threshold for a sync word search to be performed. The signal can also be observed on one of the GDO pins and in the status register bit PKTSTATUS.CS.

Other uses of Carrier Sense include the TX-If-CCA function (see section 26.4 on page 27) and the optional fast RX termination (see section 28.7 on page 32).

26.4 Clear Channel Assessment (CCA)

The Clear Channel Assessment is used to indicate if the current channel is free or busy. The current CCA state is viewable on any of GDO pins.

MCSM1.CCA_MODE selects the mode to use when determining CCA.

When the STX or SFSTXON command strobe is given while ***CC2500*** is in the RX state, the TX state is only entered if the clear channel requirements are fulfilled. The chip will otherwise remain in RX. This feature is called TX if CCA.

Four CCA requirements can be programmed:

- Always (CCA disabled, always goes to TX)
- If RSSI is below threshold
- Unless currently receiving a packet
- Both the above (RSSI below threshold and not currently receiving a packet)

26.5 Link Quality Indicator (LQI)

The Link Quality Indicator is a metric of the current quality of the received signal. If PKTCTRL1.APPEND_STATUS is enabled, the value is automatically appended to the end of each received packet. The value can also be read from the LQI status register. The LQI is calculated over the 64 symbols following the sync word (first 8 packet bytes for 2-ary modulation, first 16 packet bytes for 4-ary modulation). LQI is best used as a relative measurement of the link quality, since the value is dependent on the modulation format.

27 Forward Error Correction with Interleaving

27.1 Forward Error Correction (FEC)

CC2500 has built in support for Forward Error Correction (FEC). To enable this option, set MDMCFG1.FEC_EN to 1. FEC is employed on the data field and CRC word in order to reduce the gross bit error rate when operating near the sensitivity limit. Redundancy is added to the transmitted data in such a way that the receiver can restore the original data in the presence of some bit errors.

The use of FEC allows correct reception at a lower SNR, thus extending communication range. Alternatively, for a given SNR, using FEC decreases the bit error rate (BER). As the packet error rate (PER) is related to BER by:

$$PER = 1 - (1 - BER)^{packet\_length},$$

a lower BER can be used to allow significantly longer packets, or a higher percentage of packets of a given length, to be transmitted successfully. Finally, in realistic ISM radio environments, transient and time-varying phenomena will produce occasional errors even in otherwise good reception conditions. FEC will mask such errors and, combined with interleaving of the coded data, even correct relatively long periods of faulty reception (burst errors).

The FEC scheme adopted for ***CC2500*** is convolutional coding, in which *n* bits are generated based on *k* input bits and the *m* most recent input bits, forming a code stream able to withstand a certain number of bit errors between each coding state (the *m*-bit window).

The convolutional coder is a rate 1/2 code with a constraint length of m=4. The coder codes

one input bit and produces two output bits; hence, the effective data rate is halved.

27.2 Interleaving

Data received through real radio channels will often experience burst errors due to interference and time-varying signal strengths. In order to increase the robustness to errors spanning multiple bits, interleaving is used when FEC is enabled. After de-interleaving, a continuous span of errors in the received stream will become single errors spread apart.

CC2500 employs matrix interleaving, which is illustrated in Figure 9. The on-chip interleaving and de-interleaving buffers are 4 x 4 matrices. In the transmitter, the data bits are written into the rows of the matrix, whereas the bit sequence to be transmitted is read from the columns of the matrix and fed to the rate ½ convolutional coder. Conversely, in the receiver, the received symbols are written into the columns of the matrix, whereas the data passed onto the convolutional decoder is read from the rows of the matrix.

When FEC and interleaving is used, the amount of data transmitted over the air must be a multiple of the size of the interleaver buffer (two bytes). In addition, at least one extra byte is required for trellis termination. The packet control hardware therefore automatically inserts one or two extra bytes at the end of the packet, so that the total length of the data to be interleaved is an even number. Note that these extra bytes are invisible to the user, as they are removed before the received packet enters the RX FIFO.

Due to the implementation of the FEC and interleaver, the data to be interleaved must be at least two bytes. One byte long fixed length packets without CRC is therefore not supported when FEC/interleaving is enabled.

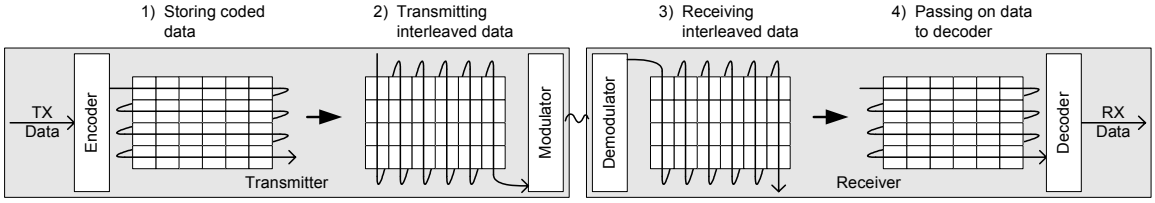

Figure 9: General principle of matrix interleaving

28 Radio Control

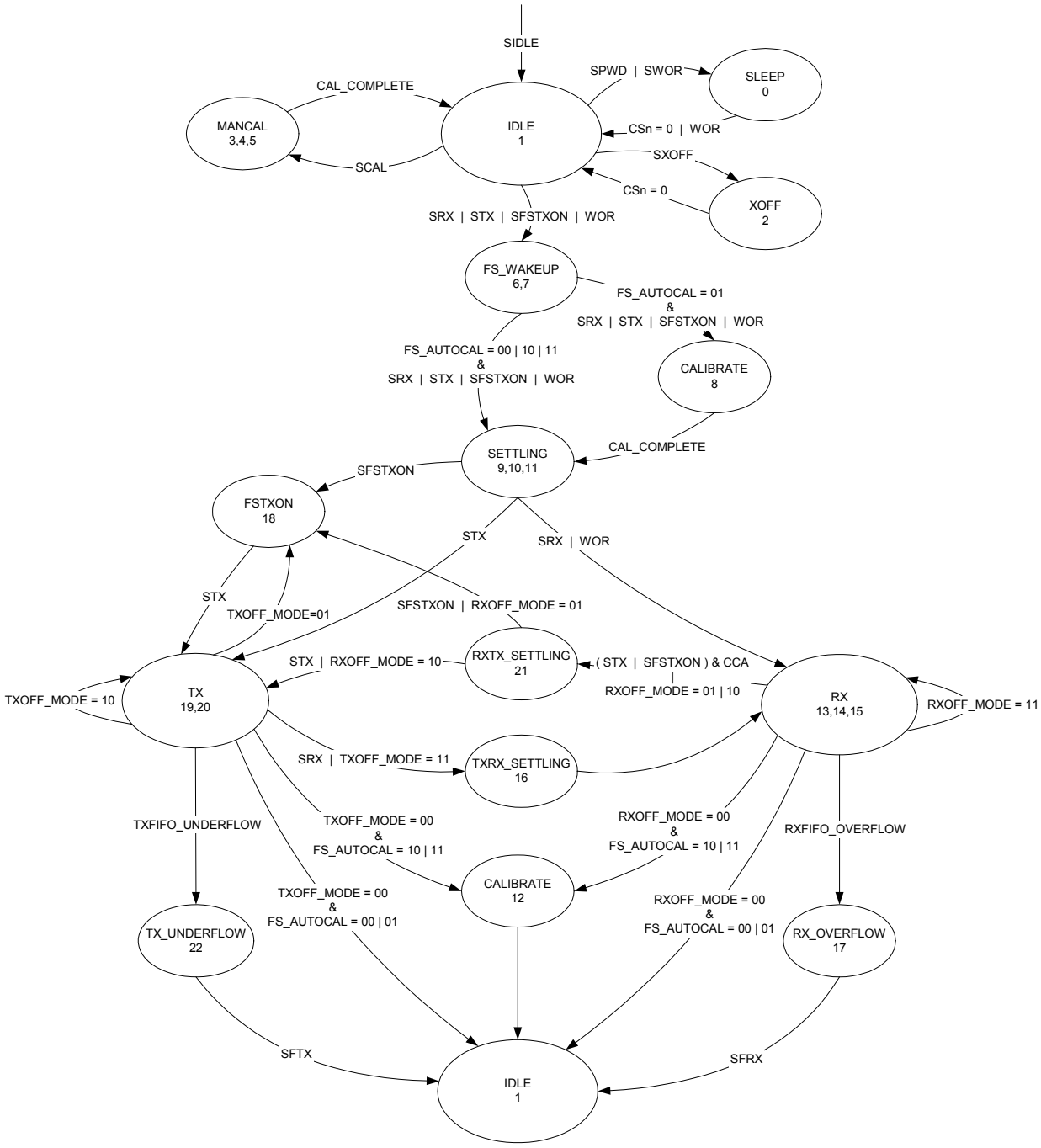

Figure 10: Complete Radio Control State Diagram

CC2500 has a built-in state machine that is used to switch between different operation states (modes). The change of state is done either by using command strobes or by internal events such as TX FIFO underflow.

A simplified state diagram, together with typical usage and current consumption, is shown in Figure 4 on page 11. The complete radio control state diagram is shown in Figure 10. The numbers refer to the state number readable in the MARCSTATE status register. This functionality is primarily for test purposes.

28.1 Power on start-up sequence

When the power supply is turned on, the system must be reset. One of the following two sequences must be followed: Automatic power-on reset or manual reset.

A power-on reset circuit is included in the ***CC2500***. The minimum requirements stated in Section 13 must be followed for the power-on reset to function properly. The internal power-up sequence is completed when CHIP_RDYn goes low. CHIP_RDYn is observed on the SO pin after CSn is pulled low. See Section 19.1 for more details on CHIP_RDYn.

The other global reset possibility on ***CC2500*** is the SRES command strobe. By issuing this strobe, all internal registers and states are set to the default, idle state. The power-up sequence is as follows (see Figure 11):

- Set SCLK=1 and SI=0, to avoid potential problems with pin control mode (see section 20.3 on page 21).
- Strobe CSn low / high.
- Hold CSn high for at least 40µs.
- Pull CSn low and wait for SO to go low (CHIP_RDYn).
- Issue the SRES strobe.
- When SO goes low again, reset is complete and the chip is in the IDLE state.

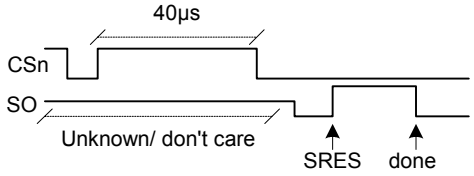

Figure 11: Power-up with SRES

It is recommended to always send a SRES command strobe on the SPI interface after power-on even though power-on reset is used.

28.2 Crystal Control

The crystal oscillator (XOSC) is either automatically controlled or always on, if MCSM0.XOSC_FORCE_ON is set.

In the automatic mode, the XOSC will be turned off if the SXOFF or SPWD command strobes are issued; the state machine then goes to XOFF or SLEEP respectively. This can be done from any state. The XOSC will be turned off when CSn is released (goes high). The XOSC will be automatically turned on again when CSn goes low. The state machine will then go to the IDLE state. The SO pin on the SPI interface must be zero before the SPI interface is ready to be used; as described in Section 0 on page 17.

If the XOSC is forced on, the crystal will always stay on even in the SLEEP state.

Crystal oscillator start-up time depends on crystal ESR and load capacitances. The electrical specification for the crystal oscillator can be found in section 8 on page 8.

28.3 Voltage Regulator Control

The voltage regulator to the digital core is controlled by the radio controller. When the chip enters the SLEEP state, which is the state with the lowest current consumption, this regulator is disabled. This occurs after CSn is released when a SPWD command strobe has been sent on the SPI interface. The chip is now in the SLEEP state. Setting CSn low again will turn on the regulator and crystal oscillator and make the chip enter the IDLE state.

When wake on radio is enabled, the WOR module will control the voltage regulator as described in Section 28.5.

28.4 Active Modes

CC2500 has two active modes: receive and transmit. These modes are activated directly by the MCU by using the SRX and STX command strobes, or automatically by Wake on Radio.

The frequency synthesizer must be calibrated regularly. ***CC2500*** has one manual calibration option (using the SCAL strobe), and three automatic calibration options, controlled by the MCSM0.FS_AUTOCAL setting:

- Calibrate when going from IDLE to either RX or TX (or FSTXON)
- Calibrate when going from either RX or TX to IDLE
- Calibrate every fourth time when going from either RX or TX to IDLE

The calibration takes a constant number of XOSC cycles (see Table 20 for timing details).

When RX is activated, the chip will remain in receive mode until the RX termination timer expires (see section 28.7) or a packet has been successfully received. After one of these events, the radio controller will go to the state indicated by the MCSM1.RXOFF_MODE setting. The possible destinations are:

- IDLE
- FSTXON: Frequency synthesizer on and ready at the TX frequency. Activate TX with STX.
- TX: Start sending preambles
- RX: Start search for a new packet

Similarly, when TX is active the chip will remain in the TX state until the current packet has been successfully transmitted. Then the state will change as indicated by the MCSM1.TXOFF_MODE setting. The possible destinations are the same as for RX.

The MCU can manually change the state from RX to TX and vice versa by using the command strobes. If the radio controller is currently in transmit and the SRX strobe is used, the current transmission will be ended and the transition to RX will be done.

If the radio controller is in RX when the STX or SFSTXON command strobes are used, the "TX if clear channel" function will be used. If the channel is not clear, the chip will remain in RX. The MCSM1.CCA_MODE setting controls the conditions for clear channel assessment. See section 26.4 on page 27 for details.

The SIDLE command strobe can always be used to force the radio controller to go to the IDLE state.

28.5 Wake on Radio (WOR)

The optional Wake on Radio (WOR) functionality enables ***CC2500*** to periodically wake up from deep sleep and listen for incoming packets without MCU interaction.

When WOR is enabled, the ***CC2500*** will go to the SLEEP state when CSn is released after the SWOR command strobe has been sent on the SPI interface. The RC oscillator must be enabled before the WOR strobe can be used, as it is the clock source for the WOR timer. The on-chip timer will get ***CC2500*** back into the IDLE state when the timer expires. After a programmable time in RX, the chip goes back to SLEEP, unless a packet is received. See section 28.7 for details on how the timeout works.

CC2500 can be set up to signal the MCU that a packet has been received by using the GDO pins. If a packet is received, the MCSM1.RXOFF_MODE will determine the behaviour at the end of the received packet. When the MCU has read the packet, it can put the chip back into SLEEP with the SWOR strobe. The FIFO will lose its contents in the SLEEP state.

The WOR timer has two events, Event 0 and Event 1. In the SLEEP state with WOR activated, reaching Event 0 will turn the digital regulator and start the crystal oscillator. Event 1 follows Event 0 after a programmed timeout.

The time between two consecutive Event 0 is programmed with a mantissa value given by WOREVT1.EVENT0 and WOREVT0.EVENT0, and an exponent value set by WORCTRL.WOR_RES. The equation is:

$$t_{Event0} = \frac{750}{f_{XOSC}} \cdot EVENT0 \cdot 2^{5 \cdot WOR\_RES}$$

The Event 1 timeout is programmed with WORCTRL.EVENT1. Figure 12 shows the timing relationship between Event 0 timeout and Event 1 timeout.

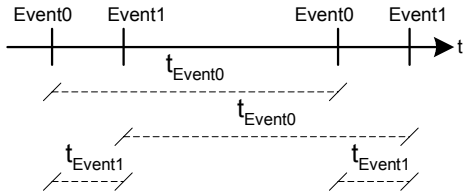

Figure 12: Event 0 and Event 1 Relationship

The WOR functionality has two control modes selected by the PKTCTRL1.WOR_AUTOSYNC bit. When this value is set to 0, the radio will wake up on Event 0 and enable RX on Event 1. This ensures that RX is entered at a precise time.

When PKTCTRL1.WOR_AUTOSYNC is set to 1, after Event 0 wakes up the chip, it will enter RX mode as soon as the chip is ready. When a sync word is detected, the WOR timer will be reset to the programmed Event 1 value. The timer will now be synchronized to the received packet. By programming Event 0 to the packet spacing time and Event 1 to a time large

enough to wake up the chip and receive a sync word, the timer will stay self-synchronized to the incoming packets.

28.5.1 RC oscillator and timing

The frequency of the low-power RC oscillator used for the WOR functionality varies with temperature and supply voltage. In order to keep the frequency as accurate as possible, the RC oscillator will be calibrated whenever possible, which is when the XOSC is running and the chip is not in the SLEEP state. When the power and XOSC is enabled, the clock used by the WOR timer is a divided XOSC clock. When the chip goes to the sleep state, the RC oscillator will use the last valid calibration result. The frequency of the RC oscillator is locked to the main crystal frequency divided by 750.

Description	XOSC periods	26MHz crystal
Idle to RX, no calibration	2298	88.4µs
Idle to RX, with calibration	~21037	809µs
Idle to TX/FSTXON, no calibration	2298	88.4µs
Idle to TX/FSTXON, with calibration	~21037	809µs
TX to RX switch	560	21.5µs
RX to TX switch	250	9.6µs
RX or TX to IDLE, no calibration	2	0.1µs
RX or TX to IDLE, with calibration	~18739	721µs
Manual calibration	~18739	721µs

Table 20: State transition timing

28.6 Timing

The radio controller controls most timing in ***CC2500***, such as synthesizer calibration, PLL lock and RT/TX turnaround times. Timing from IDLE to RX and IDLE to TX is constant, dependent on the auto calibration setting. RX/TX and TX/RX turnaround times are constant. The calibration time is constant 18739 clock periods. Table 20 shows timing in crystal clock cycles for key state transitions.

Power on time and XOSC start-up times are variable, but within the limits stated in Table 7.

28.7 RX Termination Timer

CC2500 has optional functions for automatic termination of RX after a programmable time. The main use for this functionality is wake-on-radio (WOR), but it may be useful for other applications. The termination timer starts when enabling the demodulator. The timeout is programmable with the `MCSM2.RX_TIME` setting. When the timer expires, the radio controller will check the condition for staying in RX; if the condition is not met, RX will terminate. After the timeout, the condition will be checked continuously.

The programmable conditions are:

- `MCSM2.RX_TIME_QUAL=0`: Continue receive if sync word has been found
- `MCSM2.RX_TIME_QUAL=1`: Continue receive if sync word has been found or preamble quality is above threshold (PQT)

If the system can expect the transmission to have started when enabling the receiver, the `MCSM2.RX_TIME_RSSI` function can be used. The radio controller will then terminate RX if the first valid carrier sense sample indicates no carrier (RSSI below threshold). See Section 26.3 on page 26 for details on Carrier Sense.

For ASK/OOK modulation, lack of carrier sense is only considered valid after eight symbol periods. Thus, the `MCSM2.RX_TIME_RSSI` function can be used in ASK/OOK mode when the distance between “1” symbols is 8 or less.

If RX terminates due to no carrier sense when the `MCSM2.RX_TIME_RSSI` function is used, or if no sync word was found when using the `MCSM2.RX_TIME` timeout function, the chip will always go back to IDLE. Otherwise, the `MCSM1.RXOFF_MODE` setting determines the state to go to when RX ends.

Note that in wake-on-radio (WOR) mode, the WOR state is cleared in the latter case. This means that the chip will not automatically go back to SLEEP again, even if e.g. the address field in the packet did not match. It is therefore recommended to always wake up the microcontroller on sync word detection when using WOR mode. This can be done by selecting output signal 6 (see Table 24 on page 38) on one of the programmable GDO output pins, and programming the microcontroller to wake up on an edge-triggered interrupt from this GDO pin.

29 Data FIFO

The ***CC2500*** contains two 64 byte FIFOs, one for received data and one for data to be transmitted. The SPI interface is used to read from the RX FIFO and write to the TX FIFO. Section 19.4 contains details on the SPI FIFO access. The FIFO controller will detect overflow in the RX FIFO and underflow in the TX FIFO.

When writing to the TX FIFO it is the responsibility of the MCU to avoid TX FIFO overflow. This will not be detected by the ***CC2500***.

Likewise, when reading the RX FIFO the MCU must avoid reading the RX FIFO past its empty value, since this will lead to an error that is not detected by the ***CC2500***.

The chip status byte that is available on the SO pin while transferring the SPI address contains the fill grade of the RX FIFO if the address is a read operation and the fill grade of the TX FIFO is the address is a write operation. Section 19.1 on page 17 contains more details on this.

The number of bytes in the RX FIFO and TX FIFO can also be read from the status registers `RXBYTES.NUM_RXBYTES` and `TXBYTES.NUM_TXBYTES` respectively.

The 4-bit `FIFOTHR.FIFO_THR` setting is used to program threshold points in the FIFOs. Table 21 lists the 16 `FIFO_THR` settings and the corresponding thresholds for the RX and TX FIFOs. The threshold value is coded in opposite directions for the RX FIFO and TX FIFO. This gives equal margin to the overflow and underflow conditions when the threshold is reached.

A flag will assert when the number of bytes in the FIFO is equal to or higher than the programmed threshold. The flag is used to generate the FIFO status signals that can be viewed on the GDO pins (see Section 36 on page 37).

Figure 14 shows the number of bytes in both the RX FIFO and TX FIFO when the threshold flag toggles, in the case of `FIFO_THR`=13. Figure 13 shows the flag as the respective FIFO is filled above the threshold, and then drained below.

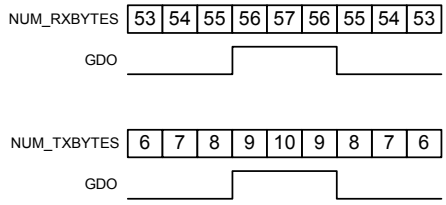

Figure 13: `FIFO_THR`=13 vs. number of bytes in FIFO

FIFO_THR	Bytes in TX FIFO	Bytes in RX FIFO
0 (0000)	61	4
1 (0001)	57	8
2 (0010)	53	12
3 (0011)	49	16
4 (0100)	45	20
5 (0101)	41	24
6 (0110)	37	28
7 (0111)	33	32
8 (1000)	29	36
9 (1001)	25	40
10 (1010)	21	44
11 (1011)	17	48
12 (1100)	13	52
13 (1101)	9	56
14 (1110)	5	60
15 (1111)	1	64

Table 21: `FIFO_THR` settings and the corresponding FIFO thresholds

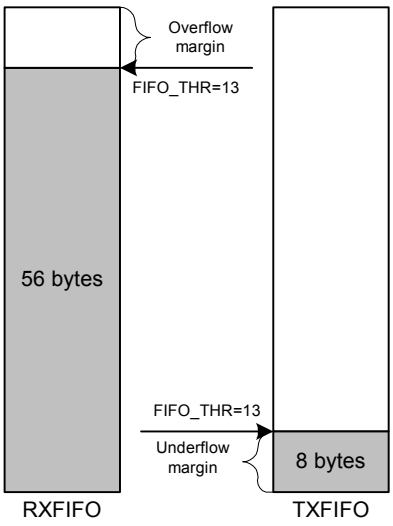

Figure 14: Example of FIFOs at threshold

30 Frequency Programming

The frequency programming in ***CC2500*** is designed to minimize the programming needed in a channel-oriented system.

To set up a system with channel numbers, the desired channel spacing is programmed with the MDMCFG0.CHANSPC_M and MDMCFG1.CHANSPC_E registers. The channel spacing registers are mantissa and exponent respectively.

The base or start frequency is set by the 24 bit frequency word located in the FREQ2, FREQ1 and FREQ0 registers. This word will typically be set to the centre of the lowest channel frequency that is to be used.

The desired channel number is programmed with the 8-bit channel number register, CHANNR.CHAN, which is multiplied by the channel offset. The resultant carrier frequency is given by:

$$f_{carrier} = \frac{f_{XOSC}}{2^{16}} \cdot \left(FREQ + CHAN \cdot \left(256 + CHANSPC\_M \cdot 2^{CHANSPC\_E-2} \right) \right)$$

The preferred IF frequency is programmed with the FSCTRL1.FREQ_IF register. The IF frequency is given by:

$$f_{IF} = \frac{f_{XOSC}}{2^{10}} \cdot FREQ\_IF$$

Note that the SmartRF® Studio software automatically calculates the optimum FSCTRL1.FREQ_IF register setting based on channel spacing and channel filter bandwidth.

If any frequency programming register is altered when the frequency synthesizer is running, the synthesizer may give an undesired response. Hence, the frequency programming should only be updated when the radio is in the IDLE state.

31 VCO

The VCO is completely integrated on-chip.

31.1 VCO and PLL Self-Calibration

The VCO characteristics will vary with temperature and supply voltage changes, as well as the desired operating frequency. In order to ensure reliable operation, ***CC2500*** includes frequency synthesizer self-calibration circuitry. This calibration should be done regularly, and must be performed after turning on power and before using a new frequency (or channel). The number of XOSC cycles for completing the PLL calibration is given in Table 20 on page 32.

The calibration can be initiated automatically or manually. The synthesizer can be automatically calibrated each time the synthesizer is turned on, or each time the synthesizer is turned off. This is configured with the MCSM0.FS_AUTOCAL register setting. In manual mode, the calibration is initiated when the SCAL command strobe is activated in the IDLE mode. The default setting is to calibrate each time the frequency synthesizer is turned on.

Note that the calibration values are maintained in sleep mode, so the calibration is still valid after waking up from sleep mode (unless supply voltage or temperature has changed significantly).

32 Voltage Regulators

CC2500 contains several on-chip linear voltage regulators, which generate the supply voltage needed by low-voltage modules. These voltage regulators are invisible to the user, and can be viewed as integral parts of the various modules. The user must however make sure

that the absolute maximum ratings and required pin voltages in Table 1 and Table 13 are not exceeded. The voltage regulator for the digital core requires one external decoupling capacitor.

Setting the CSn pin low turns on the voltage regulator to the digital core and starts the crystal oscillator. The SO pin on the SPI interface must go low before using the serial interface (setup time is TBD).

On initial power up, the MCU must set CSn low and issue the reset command strobe SRES.

If the chip is programmed to enter power-down mode, (SPWD strobe issued), the power will be turned off after CSn goes high. The power and crystal oscillator will be turned on again when CSn goes low.

The voltage regulator output should only be used for driving the ***CC2500***.

33 Output Power Programming

The RF output power level from the device has two levels of programmability, as illustrated in Figure 15. Firstly, the special PATABLE register can hold up to eight user selected output power settings. Secondly, the 3-bit FREND0.PA_POWER value selects the PATABLE entry to use. This two-level functionality provides flexible PA power ramp up and ramp down at the start and end of transmission, as well as ASK modulation shaping. In each case, all the PA power settings in the PATABLE from index 0 up to the FREND0.PA_POWER value are used.

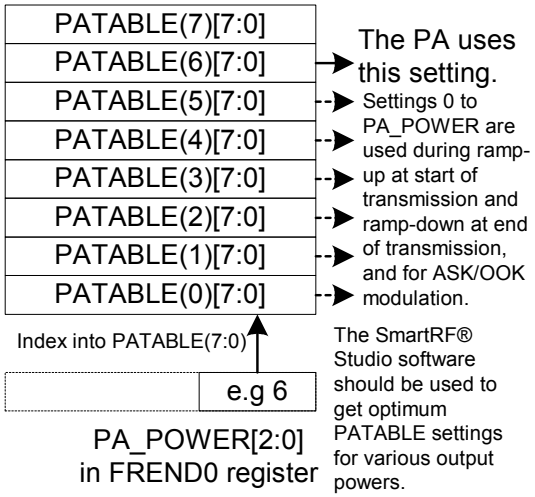

Figure 15: PA_POWER and PATABLE

The power ramping at the start and at the end of a packet can be turned off by setting FREND0.PA_POWER to zero and then programming the desired output power to index zero in the PATABLE.

Table 22 contains recommended PATABLE settings for various output levels and frequency bands. See section 19.5 on page 19 for PATABLE programming details.

With ASK modulation, the eight power settings are used for shaping. The modulator contains a counter that counts up when transmitting a one and down when transmitting a zero. The counter counts at a rate equal to 8 times the symbol rate. The counter saturates at FREND0.PA_POWER and 0 respectively. This counter value is used as an index for a lookup in the power table. Thus, in order to utilize the whole table, FREND0.PA_POWER should be 7 when ASK is active. The shaping of the ASK signal is dependent on the configuration of the PATABLE.

Output power [dBm]	Setting	Current consumption, typ. [mA]
(–55 or less)	0x00	8.9
–30	0x44	10.1
–28	0x41	10.0
–26	0x4C	11.7
–24	0x53	11.1
–22	0x83	10.9
–20	0x46	10.5
–18	0x4A	11.7
–16	0x86	11.0
–14	0x66	12.9
–12	0xC6	11.5
–10	0x69	14.1
–8	0x99	13.6
–6	0x7F	15.4
–4	0xAA	16.7
–2	0xBF	18.5
0	0xFB	21.6
1	0xFF	21.9

Table 22: Optimum PATABLE settings for various output power levels (subject to changes)

34 Crystal Oscillator

A crystal in the frequency range 26MHz-28MHz must be connected between the XOSC_Q1 and XOSC_Q2 pins. The oscillator is designed for parallel mode operation of the crystal. In addition, loading capacitors (C81 and C101) for the crystal are required. The loading capacitor values depend on the total load capacitance, C_L, specified for the crystal. The total load capacitance seen between the crystal terminals should equal C_L for the crystal to oscillate at the specified frequency.

$$C_L = \frac{1}{\frac{1}{C_{81}} + \frac{1}{C_{101}}} + C_{parasitic}$$

The parasitic capacitance is constituted by pin input capacitance and PCB stray capacitance. Total parasitic capacitance is typically 2.5pF.

The crystal oscillator circuit is shown in Figure 16. Typical component values for different values of C_L are given in Table 23.

The crystal oscillator is amplitude regulated. This means that a high current is used to start up the oscillations. When the amplitude builds up, the current is reduced to what is necessary to maintain approximately 0.4Vpp signal swing. This ensures a fast start-up, and keeps the drive level to a minimum. The ESR of the crystal should be within the specification in order to ensure a reliable start-up (see section 8 on page 8).

The initial tolerance, temperature drift, aging and load pulling should be carefully specified in order to meet the required frequency accuracy in a certain application. By specifying the *total* expected frequency accuracy in SmartRF® Studio together with data rate and frequency deviation, the software calculates the total bandwidth and compares this to the chosen receiver channel filter bandwidth. The software reports any contradictions, and a more accurate crystal is recommended if required.

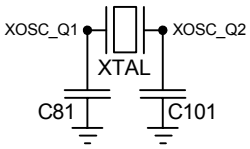

Figure 16: Crystal oscillator circuit

Component	C_L= 10pF	C_L=13pF	C_L=16pF
C81	15pF	22pF	27pF
C101	15pF	22pF	27pF

Table 23: Crystal oscillator component values

35 Antenna Interface

The balanced RF input and output of ***CC2500*** share two common pins and are designed for a simple, low-cost matching and balun network on the printed circuit board. The receive- and transmit switching at the ***CC2500*** front-end is controlled by a dedicated on-chip function, eliminating the need for an external RX/TX-switch.

A few passive external components combined with the internal RX/TX switch/termination circuitry ensures match in both RX and TX mode.

Although ***CC2500*** has a balanced RF input/output, the chip can be connected to a single-ended antenna with few external low cost capacitors and inductors.

36 General Purpose / Test Output Control Pins

The three digital output pins GDO0, GDO1 and GDO2 are general control pins configured with IOCFG0.GDO0_CFG, IOCFG1.GDO1_CFG and IOCFG2.GDO3_CFG respectively. Table 24 shows the different signals that can be monitored on the GDO pins. These signals can be used as an interrupt to the MCU. GDO1 is the same pin as the SO pin on the SPI interface, thus the output programmed on this pin will only be valid when CSn is high. The default value for GDO1 is 3-stated, which is useful when the SPI interface is shared with other devices.

The default value for GDO0 is a 125kHz-146kHz clock output (XOSC frequency divided by 192). Since the XOSC is turned on at power-on-reset, this can be used to clock the MCU in systems with only one crystal. When the MCU is up and running, it can change the clock frequency by writing to IOCFG0.GDO0_CFG. This will not produce any clock glitches.

An on-chip analog temperature sensor is enabled by writing the value 128 (0x80h) to the IOCFG0.GDO0_CFG register. The voltage on the GDO0 pin is then proportional to temperature. See section 11 on page 10 for temperature sensor specifications.

GDO0_CFG[5:0] GDO1_CFG[5:0] GDO2_CFG[5:0]	Description
0 (0x00)	Associated to the RX FIFO: Asserts when RX FIFO is filled above RXFIFO_THR. De-asserts when RX FIFO is drained below RXFIFO_THR.
1 (0x01)	Associated to the RX FIFO: Asserts when RX FIFO is filled above RXFIFO_THR or the end of packet is reached. De-asserts when RX FIFO is empty.
2 (0x02)	Associated to the TX FIFO: Asserts when the TX FIFO is filled above TXFIFO_THR. De-asserts when the TX FIFO is below TXFIFO_THR.
3 (0x03)	Associated to the TX FIFO: Asserts when TX FIFO is full. De-asserts when the TX FIFO is drained below TXFIFO_THR.
4 (0x04)	Asserts when the RX FIFO has overflowed. De-asserts when the FIFO has been flushed.
5 (0x05)	Asserts when the TX FIFO has underflowed. De-asserts when the FIFO is flushed.
6 (0x06)	Asserts when sync word has been sent / received, and de-asserts at the end of the packet. In RX, the pin will de-assert when the optional address check fails or the RX FIFO overflows. In TX the pin will de-assert if the TX FIFO underflows.
7 (0x07)	Asserts when a packet has been received with OK CRC. De-asserts when the first byte is read from the RX FIFO.
8 (0x08)	Preamble Quality Reached. Asserts when the PQI is above the programmed PQT value.
9 (0x09)	Clear channel assessment. High when RSSI level is below threshold (dependent on the current CCA_MODE setting)
10 (0x0A)	Lock detector output
11 (0x0B)	Serial Clock. Synchronous to the data in synchronous serial mode. Data is set up on the falling edge and is read on the rising edge of SERIAL_CLK.
12 (0x0C)	Serial Synchronous Data Output. Used for synchronous serial mode. The MCU must read DO on the rising edge of SERIAL_CLK. Data is set up on the falling edge by ***CC2500***.
13 (0x0D)	Serial transparent Data Output. Used for asynchronous serial mode.
14 (0x0E)	Carrier sense. High if RSSI level is above threshold.
15 (0x0F)	CRC OK. The last CRC comparison matched. Cleared when entering/restarting RX mode.
16 (0x10)	Reserved – used for test.
17 (0x11)	Reserved – used for test.
18 (0x12)	Reserved – used for test.
19 (0x13)	Reserved – used for test.
20 (0x14)	Reserved – used for test.
21 (0x15)	Reserved – used for test.
22 (0x16)	RX_HARD_DATA[1]. Can be used together with RX_SYMBOL_TICK for alternative serial RX output.
23 (0x17)	RX_HARD_DATA[0]. Can be used together with RX_SYMBOL_TICK for alternative serial RX output.
24 (0x18)	Reserved – used for test.
25 (0x19)	Reserved – used for test.
26 (0x1A)	Reserved – used for test.
27 (0x1B)	PA_PD. PA is enabled when 1, in power-down when 0. Can be used to control external PA or RX/TX switch.
28 (0x1C)	LNA_PD. LNA is enabled when 1, in power-down when 0. Can be used to control external LNA or RX/TX switch.
29 (0x1D)	RX_SYMBOL_TICK. Can be used together with RX_HARD_DATA for alternative serial RX output.
30 (0x1E)	Reserved – used for test.
31 (0x1F)	Reserved – used for test.
32 (0x20)	Reserved – used for test.
33 (0x21)	Reserved – used for test.
34 (0x22)	Reserved – used for test.
35 (0x23)	Reserved – used for test.
36 (0x24)	Reserved – used for test.
37 (0x25)	Reserved – used for test.
38 (0x26)	Reserved – used for test.
39 (0x27)	Reserved – used for test.
40 (0x28)	Reserved – used for test.
41 (0x29)	CHIP_RDY
42 (0x2A)	Reserved – used for test.
43 (0x2B)	XOSC_STABLE
44 (0x2C)	Reserved – used for test.
45 (0x2D)	GDO0_Z_EN_N. When this output is 0, GDO0 is configured as input (for serial TX data).
46 (0x2E)	High impedance (3-state)
47 (0x2F)	HW to 0 (HW1 achieved with _INV signal)
48 (0x30)	CLK_XOSC/1
49 (0x31)	CLK_XOSC/1.5
50 (0x32)	CLK_XOSC/2
51 (0x33)	CLK_XOSC/3
52 (0x34)	CLK_XOSC/4
53 (0x35)	CLK_XOSC/6
54 (0x36)	CLK_XOSC/8
55 (0x37)	CLK_XOSC/12
56 (0x38)	CLK_XOSC/16
57 (0x39)	CLK_XOSC/24
58 (0x3A)	CLK_XOSC/32
59 (0x3B)	CLK_XOSC/48
60 (0x3C)	CLK_XOSC/64
61 (0x3D)	CLK_XOSC/96
62 (0x3E)	CLK_XOSC/128
63 (0x3F)	CLK_XOSC/192

Table 24: GDO signal selection

37 Asynchronous and Synchronous Serial Operation

Several features and modes of operation have been included in the ***CC2500*** to provide backward compatibility with previous Chipcon products and other existing RF communication systems. For new systems, it is recommended to use the built-in packet handling features, as they can give more robust communication, significantly offload the microcontroller and simplify software development.

37.1 Asynchronous operation

For backward compatibility with systems already using the asynchronous data transfer from other Chipcon products, asynchronous transfer is also included in ***CC2500***. When asynchronous transfer is enabled, several of the support mechanisms for the MCU that are included in ***CC2500*** will be disabled, such as packet handling hardware, buffering in the FIFO and so on. The asynchronous transfer mode does not allow the use of the data whitener, interleaver and FEC.

Only 2-FSK and ASK/OOK are supported for asynchronous transfer.

Setting `PKTCTRL0.PKT_FORMAT` to 3 enables asynchronous transparent (serial) mode.

In TX, the `GDO0` pin is used for data input (TX data). Data output can be `GDO0`, `GDO1` or `GDO2`.

The MCU must control start and stop of transmit and receive with the `STX`, `SRX` and `SIDLE` strobes.

The ***CC2500*** modulator samples the level of the asynchronous input 8 times faster than the programmed data rate. The timing requirement for the asynchronous stream is that the error in the bit period must be less than one eighth of the programmed data rate.

37.2 Synchronous serial operation

In the Synchronous serial operation mode, data is transferred on a two wire serial interface. The ***CC2500*** provides a clock that is used to set up new data on the data input line or sample data on the data output line. Data input (TX data) is the `GDO0` pin. This pin will automatically be configured as an input when TX is active. The data output pin can be any of the GDO pins; this is set by the `IOCFG0.GDO0_CFG`, `IOCFG1.GDO1_CFG` and `IOCFG2.GDO2_CFG` fields.

Preamble and sync word insertion/detection may or may not be active, dependent on the sync mode set by the `MDMCFG3.SYNC_MODE`. If preamble and sync word is disabled, all other packet handler features and FEC should also be disabled. The MCU must then handle preamble and sync word insertion and detection in software. If preamble and sync word insertion/detection is left on, all packet handling features and FEC can be used. The ***CC2500*** will insert and detect the preamble and sync word and the MCU will only provide/get the data payload. This is equivalent to the recommended FIFO operation mode.

38 Configuration Registers

The configuration of ***CC2500*** is done by programming 8-bit registers. The configuration data based on selected system parameters are most easily found by using the SmartRF® Studio software. Complete descriptions of the registers are given in the following tables. After chip reset, all the registers have default values as shown in the tables.

There are 14 Command Strobe Registers, listed in Table 25. Accessing these registers will initiate the change of an internal state or mode. There are 47 normal 8-bit Configuration Registers, listed in Table 26. Many of these registers are for test purposes only, and need not be written for normal operation of ***CC2500***.

There are also 12 Status registers, which are listed in Table 27. These registers, which are read-only, contain information about the status of ***CC2500***.

The two FIFOs are accessed through one 8-bit register. Write operations write to the TX FIFO, while read operations read from the RX FIFO.

During the address transfer and while writing to a register or the TX FIFO, a status byte is

returned. This status byte is described in Table 17 on page 20.

Table 28 summarizes the SPI address space. The address to use is given by adding the base address to the left and the burst and read/write bits on the top. Note that the burst bit has different meaning for base addresses above and below 0x2F.

Address	Strobe Name	Description
0x30	SRES	Reset chip.
0x31	SFSTXON	Enable and calibrate frequency synthesizer (if MCSM0.FS_AUTOCAL=1). If in RX (with CCA): Go to a wait state where only the synthesizer is running (for quick RX / TX turnaround).
0x32	SXOFF	Turn off crystal oscillator.
0x33	SCAL	Calibrate frequency synthesizer and turn it off (enables quick start).
0x34	SRX	Enable RX. Perform calibration first if coming from IDLE and MCSM0.FS_AUTOCAL=1.
0x35	STX	In IDLE state: Enable TX. Perform calibration first if MCSM0.FS_AUTOCAL=1. If in RX state and CCA is enabled: Only go to TX if channel is clear.
0x36	SIDLE	Exit RX / TX, turn off frequency synthesizer and exit Wake-On-Radio mode if applicable.
0x37	SAFC	Perform AFC adjustment of the frequency synthesizer as outlined in section 23.1.
0x38	SWOR	Start automatic RX polling sequence (Wake-on-Radio) as described in section 28.5.
0x39	SPWD	Enter power down mode when CSn goes high.
0x3A	SFRX	Flush the RX FIFO buffer.
0x3B	SFTX	Flush the TX FIFO buffer.
0x3C	SWORRST	Reset real time clock.
0x3D	SNOP	No operation. May be used to pad strobe commands to two bytes for simpler software.

Table 25: Command Strobes

Address	Register	Description	Preserved in SLEEP state	Details on page number
0x00	IOCFG2	GDO2 output pin configuration	Yes	44
0x01	IOCFG1	GDO1 output pin configuration	Yes	44
0x02	IOCFG0	GDO0 output pin configuration	Yes	44
0x03	FIFOTHR	RX FIFO and TX FIFO thresholds	Yes	45
0x04	SYNC1	Sync word, high byte	Yes	45
0x05	SYNC0	Sync word, low byte	Yes	45
0x06	PKTLEN	Packet length	Yes	45
0x07	PKTCTRL1	Packet automation control	Yes	46
0x08	PKTCTRL0	Packet automation control	Yes	47
0x09	ADDR	Device address	Yes	47
0x0A	CHANNR	Channel number	Yes	47
0x0B	FSCTRL1	Frequency synthesizer control	Yes	48
0x0C	FSCTRL0	Frequency synthesizer control	Yes	48
0x0D	FREQ2	Frequency control word, high byte	Yes	48
0x0E	FREQ1	Frequency control word, middle byte	Yes	48
0x0F	FREQ0	Frequency control word, low byte	Yes	49
0x10	MDMCFG4	Modem configuration	Yes	49
0x11	MDMCFG3	Modem configuration	Yes	49
0x12	MDMCFG2	Modem configuration	Yes	50
0x13	MDMCFG1	Modem configuration	Yes	51
0x14	MDMCFG0	Modem configuration	Yes	51
0x15	DEVIATN	Modem deviation setting	Yes	51
0x16	MCSM2	Main Radio Control State Machine configuration	Yes	52
0x17	MCSM1	Main Radio Control State Machine configuration	Yes	53
0x18	MCSM0	Main Radio Control State Machine configuration	Yes	54
0x19	FOCCFG	Frequency Offset Compensation configuration	Yes	54
0x1A	BSCFG	Bit Synchronization configuration	Yes	54
0x1B	AGCTRL2	AGC control	Yes	54
0x1C	AGCTRL1	AGC control	Yes	55
0x1D	AGCTRL0	AGC control	Yes	55
0x1E	WOREVT1	High byte Event 0 timeout	Yes	55
0x1F	WOREVT0	Low byte Event 0 timeout	Yes	55
0x20	WORCTRL	Wake On Radio control	Yes	56
0x21	FREND1	Front end RX configuration	Yes	56
0x22	FREND0	Front end TX configuration	Yes	57
0x23	FSCAL3	Frequency synthesizer calibration	Yes	57
0x24	FSCAL2	Frequency synthesizer calibration	Yes	57
0x25	FSCAL1	Frequency synthesizer calibration	Yes	57
0x26	FSCAL0	Frequency synthesizer calibration	Yes	58
0x27	RCCTRL1	RC oscillator configuration	Yes	58
0x28	RCCTRL0	RC oscillator configuration	Yes	58
0x29	FSTEST	Frequency synthesizer calibration control	No	58
0x2A	PTEST	Production test	No	58
0x2B	AGCTEST	AGC test	No	58
0x2C	TEST2	Various test settings	No	58
0x2D	TEST1	Various test settings	No	59
0x2E	TEST0	Various test settings	No	59

Table 26: Configuration Registers Overview

Address	Register	Description	Details on page number
0x30 (0xF0)	PARTNUM	Part number for ***CC2500***	59
0x31 (0xF1)	VERSION	Current version number	59
0x32 (0xF2)	FREQEST	Frequency Offset Estimate	59
0x33 (0xF3)	LQI	Demodulator estimate for Link Quality	59
0x34 (0xF4)	RSSI	Received signal strength indication	60
0x35 (0xF5)	MARCSTATE	Control state machine state	60
0x36 (0xF6)	WORTIME1	High byte of WOR timer	60
0x37 (0xF7)	WORTIME0	Low byte of WOR timer	61
0x38 (0xF8)	PKTSTATUS	Current GDOx status and packet status	61
0x39 (0xF9)	VCO_VC_DAC	Current setting from PLL calibration module	61
0x3A (0xFA)	TXBYTES	Underflow and number of bytes in the TX FIFO	61
0x3B (0xFB)	RXBYTES	Overflow and number of bytes in the RX FIFO	61

Table 27: Status Registers Overview

	Write		Read		
	Single byte	Burst	Single byte	Burst	
	+0x00	+0x40	+0x80	+0xC0	
0x00	IOCFG2				R/W configuration registers, burst access possible
0x01	IOCFG1				
0x02	IOCFG0				
0x03	FIFOTHR				
0x04	SYNC1				
0x05	SYNC0				
0x06	PKTLEN				
0x07	PKTCTRL1				
0x08	PKTCTRL0				
0x09	ADDR				
0x0A	CHANNR				
0x0B	FSCTRL1				
0x0C	FSCTRL0				
0x0D	FREQ2				
0x0E	FREQ1				
0x0F	FREQ0				
0x10	MDMCFG4				
0x11	MDMCFG3				
0x12	MDMCFG2				
0x13	MDMCFG1				
0x14	MDMCFG0				
0x15	DEVIATN				
0x16	MCSM2				
0x17	MCSM1				
0x18	MCSM0				
0x19	FOCCFG				
0x1A	BSCFG				
0x1B	AGCCTRL2				
0x1C	AGCCTRL1				
0x1D	AGCCTRL0				
0x1E	WOREVT1				
0x1F	WOREVT0				
0x20	WORCTRL				
0x21	FREND1				
0x22	FREND0				
0x23	FSCAL3				
0x24	FSCAL2				
0x25	FSCAL1				
0x26	FSCAL0				
0x27	RCCTRL1				
0x28	RCCTRL0				
0x29	FSTEST				
0x2A	PTEST				
0x2B	AGCTEST				
0x2C	TEST2				
0x2D	TEST1				
0x2E	TEST0				
0x2F					
0x30	SRES		SRES	PARTNUM	Command Strobes, Status registers (read only) and multi byte registers
0x31	SFSTXON		SFSTXON	VERSION	
0x32	SXOFF		SXOFF	FREQEST	
0x33	SCAL		SCAL	LQI	
0x34	SRX		SRX	RSSI	
0x35	STX		STX	MARCSTATE	
0x36	SIDLE		SIDLE	WORTIME1	
0x37	SAFC		SAFC	WORTIME0	
0x38	SWOR		SWOR	PKTSTATUS	
0x39	SPWD		SPWD	VCO_VC_DAC	
0x3A	SFRX		SFRX	TXBYTES	
0x3B	SFTX		SFTX	RXBYTES	
0x3C	SWORRST		SWORRST		
0x3D	SNOP		SNOP		
0x3E	PATABLE	PATABLE	PATABLE	PATABLE	
0x3F	TX FIFO	TX FIFO	RX FIFO	RX FIFO	

Table 28: SPI Address Space

38.1 Configuration Register Details – Registers with preserved values in sleep state

0x00: IOCFG2 – GDO2 output pin configuration

Bit	Field Name	Reset	R/W	Description
7	Reserved		R0	
6	GDO2_INV	0	R/W	Invert output, i.e. select active low / high
5:0	GDO2_CFG[5:0]	41 (0x29)	R/W	Default is CHIP_RDY (see Table 24 on page 38)

0x01: IOCFG1 – GDO1 output pin configuration

Bit	Field Name	Reset	R/W	Description
7	GDO_DS	0	R/W	Set high (1) or low (0) output drive strength on the GDO pins.
6	GDO1_INV	0	R/W	Invert output, i.e. select active low / high
5:0	GDO1_CFG[5:0]	46 (0x2E)	R/W	Default is 3-state (see Table 24 on page 38)

0x02: IOCFG0 – GDO0 output pin configuration

Bit	Field Name	Reset	R/W	Description
7	TEMP_SENSOR_ENABLE	0	R/W	Enable analog temperature sensor. Write 0 in all other register bits when using temperature sensor.
6	GDO0_INV	0	R/W	Invert output, i.e. select active low / high
5:0	GDO0_CFG[5:0]	63 (0x3F)	R/W	Default is CLK_XOSC/192 (see Table 24 on page 38)

0x03: FIFOTHR – RX FIFO and TX FIFO thresholds

Bit	Field Name	Reset	R/W	Description
7:3	Reserved	0	R/W	Write 0 for compatibility with possible future extensions
3:0	FIFO_THR[3:0]	7 (0111)	R/W	Set the threshold for the TX FIFO and RX FIFO. The threshold is exceeded when the number of bytes in the FIFO is equal to or higher than the threshold value.

Setting	Bytes in TX FIFO	Bytes in RX FIFO
0 (0000)	61	4
1 (0001)	57	8
2 (0010)	53	12
3 (0011)	49	16
4 (0100)	45	20
5 (0101)	41	24
6 (0110)	37	28
7 (0111)	33	32
8 (1000)	29	36
9 (1001)	25	40
10 (1010)	21	44
11 (1011)	17	48
12 (1100)	13	52
13 (1101)	9	56
14 (1110)	5	60
15 (1111)	1	64

0x04: SYNC1 – Sync word, high byte

Bit	Field Name	Reset	R/W	Description
7:0	SYNC[15:8]	211 (0xD3)	R/W	8 MSB of 16-bit sync word

0x05: SYNC0 – Sync word, low byte

Bit	Field Name	Reset	R/W	Description
7:0	SYNC[7:0]	145 (0x91)	R/W	8 LSB of 16-bit sync word

0x06: PKTLEN – Packet length

Bit	Field Name	Reset	R/W	Description
7:0	PACKET_LENGTH	255 (0xFF)	R/W	Indicates the packet length when fixed length packets are enabled. If variable length packets are used, this value indicates the maximum length packets allowed.

0x07: PKTCTRL1 – Packet automation control

Bit	Field Name	Reset	R/W	Description
7:5	PQT[2:0]	0 (000)	R/W	Preamble quality estimator threshold. The preamble quality estimator increases an internal counter by one each time a bit is received that is different from the previous bit, and decreases the counter by 4 each time a bit is received that is the same as the last bit. The counter saturates at 0 and 31. A threshold of 4·PQT for this counter is used to gate sync word detection. When PQT=0 a sync word is always accepted.
4	WOR_AUTOSYNC	0	R/W	Automatically synchronize timer to received packet in wake on radio mode. When enabled the timer will automatically reset the WOR timer when a sync word is detected.
3	Reserved	0	R/W	Write 0 for compatibility with possible future extensions.
2	APPEND_STATUS	1	R/W	When enabled, two status bytes will be appended to the payload of the packet. The status bytes contain RSSI and LQI values, as well as the CRC OK flag.
1:0	ADR_CHK[1:0]	0 (00)	R/W	Controls address check configuration of received packages. Setting: 0 (00) – No address check 1 (01) – Address check, no broadcast 2 (10) – Address check, 0 (0x00) broadcast 3 (11) – Address check, 0 (0x00) and 255 (0xFF) broadcast

0x08: PKTCTRL0 – Packet automation control

Bit	Field Name	Reset	R/W	Description
7	Reserved		R0	
6	WHITE_DATA	1	R/W	Turn data whitening on / off 0: Whitening off 1: Whitening on
5:4	PKT_FORMAT[1:0]	0 (00)	R/W	Format of RX and TX data Setting: 0 (00) – Normal mode, use FIFOs for RX and TX 1 (01) – Serial Synchronous mode, used for backwards compatibility 2 (10) – Random TX mode; sends random data using PN9 generator. Used for test. Works as normal mode, setting 0 (00), in RX. 3 (11) – Asynchronous transparent mode. Data in on GDO0 and Data out on either of the GDO pins
3	CC2400_EN	0	R/W	Enable CC2400 support. Use same CRC implementation as CC2400.
2	CRC_EN	1	R/W	1: CRC calculation in TX and CRC check in RX enabled 0: CRC disabled for TX and RX
1:0	LENGTH_CONFIG[1:0]	1 (01)	R/W	Configure the packet length Setting: 0 (00) – Fixed length packets, length configured in PKTLEN register 1 (01) – Variable length packets, packet length configured by the first byte after sync word 2 (10) – Enable infinite length packets 3 (11) – Reserved

0x09: ADDR – Device address

Bit	Field Name	Reset	R/W	Description
7:0	DEVICE_ADDR[7:0]	0 (0x00)	R/W	Address used for packet filtration. Optional broadcast addresses are 0 (0x00) and 255 (0xFF).

0x0A: CHANNR – Channel number

Bit	Field Name	Reset	R/W	Description
7:0	CHAN[7:0]	0 (0x00)	R/W	The 8-bit unsigned channel number, which is multiplied by the channel spacing setting and added to the base frequency.

0x0B: FSCTRL1 – Frequency synthesizer control

Bit	Field Name	Reset	R/W	Description
7:5	Reserved		R0	
4:0	FREQ_IF[4:0]	10 (0x0A)	R/W	The desired IF frequency to employ in RX. Subtracted from FS base frequency in RX and controls the digital complex mixer in the demodulator. $f_{IF} = \frac{f_{XOSC}}{2^{10}} \cdot FREQ\_IF$ The default value gives an IF frequency of 254kHz, assuming a 26.0MHz crystal.

0x0C: FSCTRL0 – Frequency synthesizer control

Bit	Field Name	Reset	R/W	Description
7:0	FREQOFF[7:0]	0 (0x00)	R/W	Frequency offset added to the base frequency before being used by the FS. (2-complement). Resolution is $F_{XTAL}/2^{14}$ (1.5kHz-1.7kHz); range is ±186kHz to ±217kHz, dependent of XTAL frequency. The SAFC strobe command and the automatic AFC mechanism add the current FREQEST value to FREQOFF.

0x0D: FREQ2 – Frequency control word, high byte

Bit	Field Name	Reset	R/W	Description
7:6	FREQ[23:22]	1 (01)	R	FREQ[23:22] is always binary 01 (the FREQ2 register is in the range 85 to 95 with 26MHz-28MHz crystal)
5:0	FREQ[21:16]	30 (0x1E)	R/W	FREQ[23:0] is the base frequency for the frequency synthesiser in increments of $F_{XOSC}/2^{16}$. $f_{carrier} = \frac{f_{XOSC}}{2^{16}} \cdot FREQ[23:0]$ The default frequency word gives a base frequency of 2464MHz, assuming a 26.0MHz crystal. With the default channel spacing settings, the following FREQ2 values and channel numbers can be used:

FREQ2	Base frequency	Frequency range (CHAN numbers)
91 (0x5B)	2386MHz	2400.2MHz-2437MHz (71-255)
92 (0x5C)	2412MHz	2412MHz-2463MHz (0-255)
93 (0x5D)	2438MHz	2431MHz-2483.4MHz (0-227)
94 (0x5E)	2464MHz	2464MHz-2483.4MHz (0-97)

0x0E: FREQ1 – Frequency control word, middle byte

Bit	Field Name	Reset	R/W	Description
7:0	FREQ[15:8]	196 (0xC4)	R/W	Ref. FREQ2 register

0x0F: FREQ0 – Frequency control word, low byte

Bit	Field Name	Reset	R/W	Description
7:0	FREQ[7:0]	236 (0xEC)	R/W	Ref. FREQ2 register

0x10: MDMCFG4 – Modem configuration

Bit	Field Name	Reset	R/W	Description
7:6	CHANBW_E[1:0]	2 (10)	R/W	
5:4	CHANBW_M[1:0]	0 (00)	R/W	Sets the decimation ratio for the delta-sigma ADC input stream and thus the channel bandwidth. $BW_{channel} = \frac{f_{XOSC}}{8 \cdot (4 + CHANBW\_M) \cdot 2^{CHANBW\_E}}$ Note that the combination CHANBW_E=0 and CHANBW_M=0 is not supported. The default values give 203kHz channel filter bandwidth, assuming a 26.0MHz crystal.
3:0	DRATE_E[3:0]	12 (1100)	R/W	The exponent of the user specified symbol rate

0x11: MDMCFG3 – Modem configuration

Bit	Field Name	Reset	R/W	Description
7:0	DRATE_M[7:0]	34 (0x22)	R/W	The mantissa of the user specified symbol rate. The symbol rate is configured using an unsigned, floating-point number with 9-bit mantissa and 4-bit exponent. The 9th bit is a hidden '1'. The resulting data rate is: $R_{DATA} = \frac{(256 + DRATE\_M) \cdot 2^{DRATE\_E}}{2^{28}} \cdot f_{XOSC}$ The default values give a data rate of 115.051kbps (closest setting to 115.2kbps), assuming a 26.0MHz crystal.

0x12: MDMCFG2 – Modem configuration

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th>Description</th></tr>
<tr><td>7</td><td>Reserved</td><td></td><td>R0</td><td></td></tr>
<tr><td>6:4</td><td>MOD_FORMAT[2:0]</td><td>1 (001)</td><td>R/W</td><td>The modulation format of the radio signal
<table>
<tr><td>Setting</td><td>Modulation format</td></tr>
<tr><td>0 (000)</td><td>2-FSK</td></tr>
<tr><td>1 (001)</td><td>-</td></tr>
<tr><td>2 (010)</td><td>-</td></tr>
<tr><td>3 (011)</td><td>ASK/OOK</td></tr>
<tr><td>4 (100)</td><td>-</td></tr>
<tr><td>5 (101)</td><td>-</td></tr>
<tr><td>6 (110)</td><td>-</td></tr>
<tr><td>7 (111)</td><td>MSK</td></tr>
</table></td></tr>
<tr><td>3</td><td>MANCHESTER_EN</td><td>0</td><td>R/W</td><td>Enables Manchester encoding/decoding.</td></tr>
<tr><td>2:0</td><td>SYNC_MODE[2:0]</td><td>2 (010)</td><td>R/W</td><td>Combined sync-word qualifier mode.

The values 0 (000) and 4 (100) disables sync word transmission in TX and sync word detection in RX.

The values 1 (001), 2 (001), 5 (101) and 6 (110) enables 16-bit sync word transmission in TX and 16-bits sync word detection in RX. Only 15 of 16 bits need to match in RX when using setting 1 (001) or 5 (101). The values 3 (011) and 7 (111) enables repeated sync word transmission in RX and 32-bits sync word detection in RX (only 30 of 32 bits need to match).
<table>
<tr><td>Setting</td><td>Sync-word qualifier mode</td></tr>
<tr><td>0 (000)</td><td>No preamble/sync</td></tr>
<tr><td>1 (001)</td><td>15/16 sync word bits detected</td></tr>
<tr><td>2 (010)</td><td>16/16 sync word bits detected</td></tr>
<tr><td>3 (011)</td><td>30/32 sync word bits detected</td></tr>
<tr><td>4 (100)</td><td>No preamble/sync, carrier-sense above threshold</td></tr>
<tr><td>5 (101)</td><td>15/16 + carrier-sense above threshold</td></tr>
<tr><td>6 (110)</td><td>16/16 + carrier-sense above threshold</td></tr>
<tr><td>7 (111)</td><td>30/32 + carrier-sense above threshold</td></tr>
</table></td></tr>
</table>

0x13: MDMCFG1 – Modem configuration

Bit	Field Name	Reset	R/W	Description
7	FEC_EN	0	R/W	Enable Forward Error Correction (FEC) with interleaving for packet payload
6:4	NUM_PREAMBLE[2:0]	2 (010)	R/W	Sets the minimum number of preamble bytes to be transmitted Setting / Number of preamble bytes 0 (000) 2 1 (001) 3 2 (010) 4 3 (011) 6 4 (100) 8 5 (101) 12 6 (110) 16 7 (111) 24
3:2	Reserved		R0	
1:0	CHANSPC_E[1:0]	2 (10)	R/W	2 bit exponent of channel spacing

0x14: MDMCFG0 – Modem configuration

Bit	Field Name	Reset	R/W	Description
7:0	CHANSPC_M[7:0]	248 (0xF8)	R/W	8-bit mantissa of channel spacing (initial 1 assumed). The channel spacing is multiplied by the channel number CHAN and added to the base frequency. It is unsigned and has the format: $\Delta f_{CHANNEL} = \frac{f_{XOSC}}{2^{18}} \cdot (256 + CHANSPC\_M) \cdot 2^{CHANSPC\_E} \cdot CHAN$ The default values give 199.951kHz channel spacing (the closest setting to 200kHz), assuming 26.0MHz crystal frequency.

0x15: DEVIATN – Modem deviation setting

Bit	Field Name	Reset	R/W	Description
7	Reserved		R0	
6:4	DEVIATION_E[2:0]	4 (100)	R/W	Deviation exponent
3	Reserved		R0	
2:0	DEVIATION_M[2:0]	7 (111)	R/W	When MSK modulation is enabled: Sets fraction of symbol period used for phase change. When FSK modulation is enabled: Deviation mantissa, interpreted as a 4-bit value with MSB implicit 1. The resulting FSK deviation is given by: $f_{dev} = \frac{f_{XOSC}}{2^{17}} \cdot (8 + DEVIATION\_M) \cdot 2^{DEVIATION\_E}$ The default values give ±47.607kHz deviation, assuming 26.0MHz crystal frequency.

0x16: MCSM2 – Main Radio Control State Machine configuration

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th>Description</th></tr>
<tr><td>7:5</td><td>Reserved</td><td></td><td>R0</td><td>Reserved</td></tr>
<tr><td>4</td><td>RX_TIME_RSSI</td><td>0</td><td>R/W</td><td>Direct RX termination based on RSSI measurement (carrier sense). For ASK/OOK modulation, RX times out if there is no carrier sense in the first 8 symbol periods.</td></tr>
<tr><td>3</td><td>RX_TIME_QUAL</td><td>0</td><td>R/W</td><td>When the RX_TIME timer expires, the chip checks if sync word is found when RX_TIME_QUAL=0, or either sync word is found or PQI is set when RX_TIME_QUAL=1.</td></tr>
<tr><td>2:0</td><td>RX_TIME[2:0]</td><td>7 (111)</td><td>R/W</td><td>Timeout for sync word search in RX. The timeout is relative to the programmed EVENT0 timeout, which means that the duty cycle can be set in wake-on-radio (WOR) mode. The RX timeout is scaled by 1 bit less than the EVENT0 timeout with respect to the WORCTRL.WOR_RES setting, as very long timeouts probably also will use very low RX duty cycles.
<table>
<tr><th>Setting</th><th>RX timeout</th><th>Duty cycle, WOR</th></tr>
<tr><td>0 (000)</td><td>$T_{EVENT0} / 2^{(3+WOR\_RES)}$</td><td>$12.5\% / 2^{WOR\_RES}$</td></tr>
<tr><td>1 (001)</td><td>$T_{EVENT0} / 2^{(4+WOR\_RES)}$</td><td>$6.25\% / 2^{WOR\_RES}$</td></tr>
<tr><td>2 (010)</td><td>$T_{EVENT0} / 2^{(5+WOR\_RES)}$</td><td>$3.125\% / 2^{WOR\_RES}$</td></tr>
<tr><td>3 (011)</td><td>$T_{EVENT0} / 2^{(6+WOR\_RES)}$</td><td>$1.563\% / 2^{WOR\_RES}$</td></tr>
<tr><td>4 (100)</td><td>$T_{EVENT0} / 2^{(7+WOR\_RES)}$</td><td>$0.781\% / 2^{WOR\_RES}$</td></tr>
<tr><td>5 (101)</td><td>$T_{EVENT0} / 2^{(8+WOR\_RES)}$</td><td>$0.391\% / 2^{WOR\_RES}$</td></tr>
<tr><td>6 (110)</td><td>$T_{EVENT0} / 2^{(9+WOR\_RES)}$</td><td>$0.195\% / 2^{WOR\_RES}$</td></tr>
<tr><td>7 (111)</td><td>Until end of packet</td><td>N/A (no timeout)</td></tr>
</table>
Note that the RC oscillator must be enabled in order to use setting 0-6, because the timeout counts RC oscillator periods. WOR mode does not need to be enabled.
The timeout counter resolution is limited: With RX_TIME=0, the timeout count is given by the 13MSBs of EVENT0, decreasing to the 7MSBs of EVENT0 with RX_TIME=6.</td></tr>
</table>

0x17: MCSM1 – Main Radio Control State Machine configuration

Bit	Field Name	Reset	R/W	Description
7:6	Reserved		R0	
5:4	CCA_MODE[1:0]	3 (11)	R/W	Selects CCA_MODE; Reflected in CCA signal Setting: 0 (00) – Always 1 (01) – If RSSI below threshold 2 (10) – Unless currently receiving a packet 3 (11) – If RSSI below threshold unless currently receiving a packet
3:2	RXOFF_MODE[1:0]	0 (00)	R/W	Select what should happen when a packet has been received Setting: 0 (00) – IDLE 1 (01) – FSTXON 2 (10) – TX 3 (11) – Stay in RX
1:0	TXOFF_MODE[1:0]	0 (00)	R/W	Select what should happen when a packet has been sent (TX) Setting: 0 (00) – IDLE 1 (01) – FSTXON 2 (10) – Stay in TX (start sending preamble) 3 (11) – RX

0x18: MCSM0 – Main Radio Control State Machine configuration

Bit	Field Name	Reset	R/W	Description
7:6	Reserved		R0	
5:4	FS_AUTOCAL[1:0]	0 (00)	R/W	Automatically calibrate when going to RX or TX, or back to IDLE Setting: 0 (00) – Never (manually calibrate using SCAL strobe) 1 (01) – When going from IDLE to RX or TX (or FSTXON) 2 (10) – When going from RX or TX back to IDLE 3 (11) – Every 4th time when going from RX or TX to IDLE In some automatic wake-on-radio (WOR) applications, using setting 3 (11) can significantly reduce current consumption.
3:2	PO_TIMEOUT	2 (10)	R/W	Programs the number of times the six-bit ripple counter must expire before CHP_RDY_N goes low. Values other than 0 (00) are most useful when the XOSC is left on during power-down. 0 (00) – Expire count 1 – Approx. 2.3µs – 2.7µs 1 (01) – Expire count 16 – Approx. 37µs – 43µs 2 (10) – Expire count 64 – Approx. 146µs – 171µs 3 (11) – Expire count 256 – Approx. 585µs – 683µs Exact timeout depends on crystal frequency.
1	PIN_CTRL_EN	0	R/W	Enables the pin radio control option
0	XOSC_FORCE_ON	0	R/W	Force the XOSC to stay on in the SLEEP state.

0x19: FOCCFG – Frequency Offset Compensation configuration

Bit	Field Name	Reset	R/W	Description
7:6	Reserved		R0	
5:0	FOCCFG[5:0]	54 (0x36)	R/W	Frequency offset compensation configuration. The value to use in this register is given by the SmartRF® Studio software.

0x1A: BSCFG – Bit Synchronization configuration

Bit	Field Name	Reset	R/W	Description
7:0	BSCFG[7:0]	108 (0x6C)	R/W	Bit Synchronization configuration. The value to use in this register is given by the SmartRF® Studio software.

0x1B: AGCCTRL2 – AGC control

Bit	Field Name	Reset	R/W	Description
7:0	AGCCTRL2[7:0]	3 (0x03)	R/W	AGC control register. The value to use in this register is given by the SmartRF® Studio software.

0x1C: AGCCTRL1 – AGC control

Bit	Field Name	Reset	R/W	Description
7	Reserved		R0	
6:0	AGCCTRL1[6:0]	64 (0x40)	R/W	AGC control register. The value to use in this register is given by the SmartRF® Studio software.

0x1D: AGCCTRL0 – AGC control

Bit	Field Name	Reset	R/W	Description
7:0	AGCCTRL0[7:0]	145 (0x91)	R/W	AGC control register. The value to use in this register is given by the SmartRF® Studio software.

0x1E: WOREVT1 – High byte event0 timeout

Bit	Field Name	Reset	R/W	Description
7:0	EVENT0[15:8]	135 (0x87)	R/W	High byte of Event 0 timeout register $t_{Event0} = \frac{750}{f_{XOSC}} \cdot EVENT0 \cdot 2^{5 \cdot WOR\_RES}$

0x1F: WOREVT0 – Low byte event0 timeout

Bit	Field Name	Reset	R/W	Description
7:0	EVENT0[7:0]	107 (0x6B)	R/W	Low byte of Event 0 timeout register. The default Event 0 value gives 1.0s timeout, assuming a 26.0MHz crystal.

0x20: WORCTRL – Wake On Radio control

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th>Description</th></tr>
<tr><td>7</td><td>RC_PD</td><td>1</td><td>R/W</td><td>Power down signal to RC oscillator. When written to 0, automatic initial calibration will be performed</td></tr>
<tr><td>6:4</td><td>EVENT1[2:0]</td><td>7 (111)</td><td>R/W</td><td>Timeout setting from register block. Decoded to Event 1 timeout. RC oscillator clock frequency equals F_{XOSC}/750, which is 32khz-37kHz, depending on crystal frequency. The table below lists the number of clock periods after Event 0 before Event 1 times out.
<table>
<tr><th>Setting</th><th>WOR_AUTOSYNC=0</th><th>WOR_AUTOSYNC=1</th></tr>
<tr><td>0 (000)</td><td>4 (0.107ms – 0.125ms)</td><td>16 (0.429ms – 0.5ms)</td></tr>
<tr><td>1 (001)</td><td>6 (0.161ms – 0.188ms)</td><td>24 (0.643ms – 0.75ms)</td></tr>
<tr><td>2 (010)</td><td>8 (0.214ms – 0.25ms)</td><td>32 (0.857ms – 1ms)</td></tr>
<tr><td>3 (011)</td><td>12 (0.321ms – 0.375ms)</td><td>48 (1.286ms – 1.5ms)</td></tr>
<tr><td>4 (100)</td><td>16 (0.429ms – 0.5ms)</td><td>64 (1.7ms – 2ms)</td></tr>
<tr><td>5 (101)</td><td>24 (0.643ms – 0.75ms)</td><td>96 (2.6ms – 3ms)</td></tr>
<tr><td>6 (110)</td><td>32 (0.857ms – 1ms)</td><td>128 (3.4ms – 4ms)</td></tr>
<tr><td>7 (111)</td><td>48 (1.286ms – 1.5ms)</td><td>192 (5.1ms – 6ms)</td></tr>
</table></td></tr>
<tr><td>3</td><td>RC_CAL</td><td>1</td><td>R/W</td><td>Enables (1) or disables (0) the RC oscillator calibration.
Included for debug/test purposes only.</td></tr>
<tr><td>2</td><td>Reserved</td><td></td><td>R0</td><td></td></tr>
<tr><td>1:0</td><td>WOR_RES</td><td>0 (00)</td><td>R/W</td><td>Controls the Event 0 resolution and maximum timeout of the WOR module:
<table>
<tr><th>Setting</th><th>Resolution (1 LSB)</th><th>Max timeout</th></tr>
<tr><td>0 (00)</td><td>1 period (27µs – 31µs)</td><td>1.8 – 2.0 seconds</td></tr>
<tr><td>1 (01)</td><td>2^5 periods (0.86ms – 1.0ms)</td><td>56 – 66 seconds</td></tr>
<tr><td>2 (10)</td><td>2^{10} periods (27ms – 32ms)</td><td>30 – 35 minutes</td></tr>
<tr><td>3 (11)</td><td>2^{15} periods (0.88s – 1.0s)</td><td>16 – 18 hours</td></tr>
</table>
Adjusting the resolution does not affect the resolution of the WOR time readout registers <code>WORTIME1</code>/<code>WORTIME0</code>.</td></tr>
</table>

0x21: FREND1 – Front end RX configuration

Bit	Field Name	Reset	R/W	Description
7:0	FREND1[7:0]	166 (0xA6)	R/W	Front end RX configuration. The value to use in this register is given by the SmartRF® Studio software.

0x22: FREND0 – Front end TX configuration

Bit	Field Name	Reset	R/W	Description
7:6	Reserved		R0	
5:4	LODIV_BUF_CURRENT_TX[1:0]	1 (01)	R/W	Adjusts current TX LO buffer (input to PA). The value to use in this field is given by the SmartRF® Studio software.
3	Reserved		R0	
2:0	PA_POWER[2:0]	0 (000)	R/W	Selects PA power setting. This value is an index to the PATABLE, which can be programmed with up to 8 different PA settings. In ASK mode, this selects the PATABLE index to use when transmitting a '1'. PATABLE index zero is used in ASK when transmitting a '0'. The PATABLE settings from index '0' to the PA_POWER value are used for ASK TX shaping, and for power ramp-up/ramp-down at the start/end of transmission in all TX modulation formats.

0x23: FSCAL3 – Frequency synthesizer calibration

Bit	Field Name	Reset	R/W	Description
7:0	FSCAL3[7:0]	169 (0xA9)	R/W	Frequency synthesizer calibration configuration and result register. The value to write in this register before calibration is given by the SmartRF® Studio software. Fast frequency hopping without calibration for each hop can be done by calibrating upfront for each frequency and saving the resulting FSCAL3, FSCAL2 and FSCAL1 register values. Between each frequency hop, calibration can be replaced by writing the FSCAL3, FSCAL2 and FSCAL1 register values corresponding to the next RF frequency.

0x24: FSCAL2 – Frequency synthesizer calibration

Bit	Field Name	Reset	R/W	Description
7:6	Reserved		R0	
5:0	FSCAL2[5:0]	10 (0x0A)	R/W	Frequency synthesizer calibration result register. Fast frequency hopping without calibration for each hop can be done by calibrating upfront for each frequency and saving the resulting FSCAL3, FSCAL2 and FSCAL1 register values. Between each frequency hop, calibration can be replaced by writing the FSCAL3, FSCAL2 and FSCAL1 register values corresponding to the next RF frequency.

0x25: FSCAL1 – Frequency synthesizer calibration

Bit	Field Name	Reset	R/W	Description
7:6	Reserved		R0	
5:0	FSCAL1[5:0]	32 (0x20)	R/W	Frequency synthesizer calibration result register. Fast frequency hopping without calibration for each hop can be done by calibrating upfront for each frequency and saving the resulting FSCAL3, FSCAL2 and FSCAL1 register values. Between each frequency hop, calibration can be replaced by writing the FSCAL3, FSCAL2 and FSCAL1 register values corresponding to the next RF frequency.

0x26: FSCAL0 – Frequency synthesizer calibration

Bit	Field Name	Reset	R/W	Description
7	Reserved		R0	
4:0	FSCAL0[6:0]	13 (0x0D)	R/W	Frequency synthesizer calibration control. The value to use in this register is given by the SmartRF® Studio software.

0x27: RCCTRL1 – RC oscillator configuration

Bit	Field Name	Reset	R/W	Description
7	Reserved	0	R0	
6:0	RCCTRL1[6:0]	65 (0x41)	R/W	RC oscillator configuration. Do not write to this register.

0x28: RCCTRL0 – RC oscillator configuration

Bit	Field Name	Reset	R/W	Description
7:6	Reserved	0	R0	
5:0	RCCTRL0[5:0]	0 (0x00)	R/W	RC oscillator configuration. Do not write to this register.

38.2 Configuration Register Details – Registers that lose programming in sleep state

0x29: FSTEST – Frequency synthesizer calibration control

Bit	Field Name	Reset	R/W	Description
7:0	FSTEST[7:0]	87 (0x57)	R/W	For test only. Do not write to this register.

0x2A: PTEST – Production test

Bit	Field Name	Reset	R/W	Description
7	PTEST[7:0]	127 (0x7F)	R/W	Writing 0xBF to this register makes the on-chip temperature sensor available in the IDLE state. The default 0x7F value should then be written back before leaving the IDLE state. Other use of this register is for test only.

0x2B: AGCTEST – AGC test

Bit	Field Name	Reset	R/W	Description
7:0	AGCTEST[7:0]	63 (0x3F)	R/W	For test only. Do not write to this register.

0x2C: TEST2 – Various test settings

Bit	Field Name	Reset	R/W	Description
7:0	TEST2[7:0]	152 (0x98)	R/W	For test only. Do not write to this register.

0x2D: TEST1 – Various test settings

Bit	Field Name	Reset	R/W	Description
7:0	TEST1[7:0]	49 (0x31)	R/W	For test only. Do not write to this register.

0x2E: TEST0 – Various test settings

Bit	Field Name	Reset	R/W	Description
7:0	TEST0[7:0]	11 (0x0B)	R/W	For test only. Do not write to this register.

38.3 Status register details

0x30 (0xF0): PARTNUM – Chip ID

Bit	Field Name	Reset	R/W	Description
7:0	PARTNUM[7:0]	128 (0x80)	R	Chip part number

0x31 (0xF1): VERSION – Chip ID

Bit	Field Name	Reset	R/W	Description
7:0	VERSION[7:0]	1 (0x01)	R	Chip version number.

0x32 (0xF2): FREQEST – Frequency Offset Estimate from demodulator

Bit	Field Name	Reset	R/W	Description
7:0	FREQOFF_EST		R	The estimated frequency offset (two's complement) of the carrier. Resolution is $F_{XTAL}/2^{14}$ (1.5kHz-1.7kHz); range is ±186kHz to ±217kHz, dependent of XTAL frequency. Frequency offset compensation is only supported for FSK and MSK modulation. This register will read 0 when using ASK or OOK modulation.

0x33 (0xF3): LQI – Demodulator estimate for Link Quality

Bit	Field Name	Reset	R/W	Description
7	CRC OK		R	The last CRC comparison matched. Cleared when entering/restarting RX mode.
6:0	LQI_EST[6:0]		R	The Link Quality Indicator estimates how easily a received signal can be demodulated. Calculated over the 64 symbols following the sync word (first 8 packet bytes for 2-ary modulation, first 16 packet bytes for 4-ary modulation).

0x34 (0xF4): RSSI – Received signal strength indication

Bit	Field Name	Reset	R/W	Description
7:0	RSSI		R	Received signal strength indicator

0x35 (0xF5): MARCSTATE – Main Radio Control State Machine state

Bit	Field Name	Reset	R/W	Description
7:5	Reserved		R0	
4:0	MARC_STATE[4:0]		R	Main Radio Control FSM State

Value	State name	State (Figure 10, page 29)
0 (0x00)	SLEEP	SLEEP
1 (0x01)	IDLE	IDLE
2 (0x02)	XOFF	XOFF
3 (0x03)	VCOON_MC	MANCAL
4 (0x04)	REGON_MC	MANCAL
5 (0x05)	MANCAL	MANCAL
6 (0x06)	VCOON	FS_WAKEUP
7 (0x07)	REGON	FS_WAKEUP
8 (0x08)	STARTCAL	CALIBRATE
9 (0x09)	BWBOOST	SETTLING
10 (0x0A)	FS_LOCK	SETTLING
11 (0x0B)	IFADCON	SETTLING
12 (0x0C)	ENDCAL	CALIBRATE
13 (0x0D)	RX	RX
14 (0x0E)	RX_END	RX
15 (0x0F)	RX_RST	RX
16 (0x10)	TXRX_SWITCH	TXRX_SETTLING
17 (0x11)	RX_OVERFLOW	RX_OVERFLOW
18 (0x12)	FSTXON	FSTXON
19 (0x13)	TX	TX
20 (0x14)	TX_END	TX
21 (0x15)	RXTX_SWITCH	RXTX_SETTLING
22 (0x16)	TX_UNDERFLOW	TX_UNDERFLOW

0x36 (0xF6): WORTIME1 – High byte of WOR time

Bit	Field Name	Reset	R/W	Description
7:0	TIME[15:8]		R	High byte of timer value in WOR module

0x37 (0xF7): WORTIME0 – Low byte of WOR time

Bit	Field Name	Reset	R/W	Description
7:0	TIME[7:0]		R	Low byte of timer value in WOR module

0x38 (0xF8): PKTSTATUS – Current GDOx status and packet status

Bit	Field Name	Reset	R/W	Description
7	CRC_OK		R	The last CRC comparison matched. Cleared when entering/restarting RX mode.
6	CS		R	Carrier sense
5	PQT_REACHED		R	Preamble Quality reached
4	CCA		R	Clear channel assessment
3	SFD		R	Sync word found
2	GDO2		R	Current value on GDO2 pin
1	GDO1		R	Current value on GDO1 pin
0	GDO0		R	Current value on GDO0 pin

0x39 (0xF9): VCO_VC_DAC – Current setting from PLL calibration module

Bit	Field Name	Reset	R/W	Description
7:0	VCO_VC_DAC[7:0]		R	Status register for test only.

0x3A (0xFA): TXBYTES – Underflow and number of bytes

Bit	Field Name	Reset	R/W	Description
7	TXFIFO_UNDERFLOW		R	
6:0	NUM_TXBYTES		R	Number of bytes in TX FIFO

0x3B (0xFB): RXBYTES – Overflow and number of bytes

Bit	Field Name	Reset	R/W	Description
7	RXFIFO_OVERFLOW		R	
6:0	NUM_RXBYTES		R	Number of bytes in RX FIFO

39 Package Description (QLP 20)

All dimensions are in millimetres, angles in degrees. NOTE: The ***CC2500*** is available in RoHS lead-free package only.

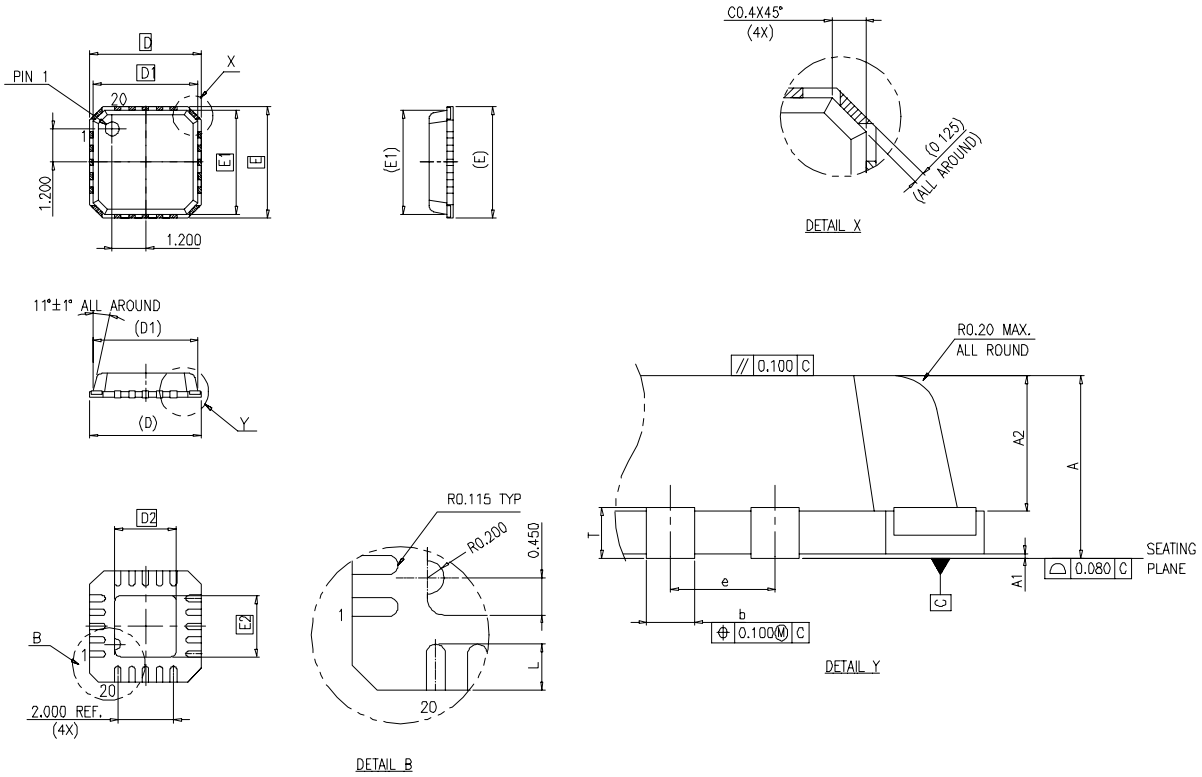

Figure 17: Package dimensions drawing

Package type		A	A1	A2	D	D1	D2	E	E1	E2	L	T	b	e
QLP 20 (4x4)	Min	0.75	0.005	0.55	3.90	3.65		3.90	3.65		0.45	0.190	0.18	
	Typ.	0.85	0.025	0.65	4.00	3.75	2.40	4.00	3.75	2.40	0.55		0.23	0.50
	Max	0.95	0.045	0.75	4.10	3.85		4.10	3.85		0.65	0.245	0.30	

Table 29: Package dimensions

39.1 Recommended PCB layout for package (QLP 20)

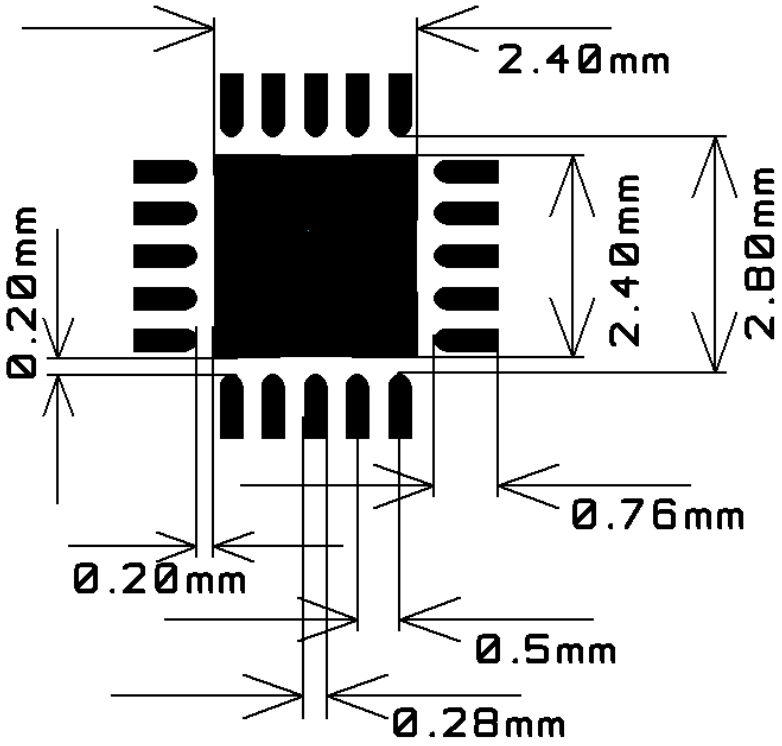

Figure 18: Recommended PCB layout for QLP 20 package

Note: The figure is an illustration only and not to scale. There are five TBD mil diameter via holes distributed symmetrically in the ground pad under the package. See also the ***CC2500*** EM reference design.

39.2 Package thermal properties

Thermal resistance	
Air velocity [m/s]	0
Rth,j-a [K/W]	TBD

Table 30: Thermal properties of QLP 20 package

39.3 Soldering information

The recommendations for lead-free reflow in IPC/JEDEC J-STD-020C should be followed.

39.4 Tray specification

CC2500 can be delivered in standard QLP 4x4mm shipping trays.

Tray Specification				
Package	Tray Width	Tray Height	Tray Length	Units per Tray
QLP 20	125.9mm	7.62mm	322.6mm	490

Table 31: Tray specification

39.5 Carrier tape and reel specification

Carrier tape and reel is in accordance with EIA Specification 481.

Tape and Reel Specification					
Package	Tape Width	Component Pitch	Hole Pitch	Reel Diameter	Units per Reel
QLP 20	TBD	TBD	TBD	13 inches	2500

Table 32: Carrier tape and reel specification

40 Ordering Information

Ordering part number	Description	Minimum Order Quantity (MOQ)
1167	***CC2500***- RTY1 QLP20 RoHS Pb-free 490/tray	490 (tray)
1190	***CC2500***- RTR1 QLP20 RoHS Pb-free 2500/T&R	2500 (tape and reel)
1192	***CC2500*** SK Sample kit 5pcs.	1
10069	***CC2500_CC2550*** DK Development Kit	1

Table 33: Ordering Information

41 General Information

41.1 Document History

Revision	Date	Description/Changes
1.0	2005-01-24	First preliminary release.

Table 34: Document history

41.2 Product Status Definitions

Data Sheet Identification	Product Status	Definition
Advance Information	Planned or Under Development	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	Engineering Samples and First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. Chipcon reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains the final specifications. Chipcon reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by Chipcon. The data sheet is printed for reference information only.

Table 35: Product Status Definitions

41.3 Disclaimer

Chipcon AS believes the information contained herein is correct and accurate at the time of this printing. However, Chipcon AS reserves the right to make changes to this product without notice. Chipcon AS does not assume any responsibility for the use of the described product; neither does it convey any license under its patent rights, or the rights of others. The latest updates are available at the Chipcon website or by contacting Chipcon directly.

As far as possible, major changes of product specifications and functionality, will be stated in product specific Errata Notes published at the Chipcon website. Customers are encouraged to sign up to the Developers Newsletter for the most recent updates on products and support tools.

When a product is discontinued this will be done according to Chipcon's procedure for obsolete products as described in Chipcon's Quality Manual. This includes informing about last-time-buy options. The Quality Manual can be downloaded from Chipcon's website.

Compliance with regulations is dependent on complete system performance. It is the customer's responsibility to ensure that the system complies with regulations.

41.4 Trademarks

SmartRF® is a registered trademark of Chipcon AS. SmartRF® is Chipcon's RF technology platform with RF library cells, modules and design expertise. Based on SmartRF® technology Chipcon develops standard component RF circuits as well as full custom ASICs based on customer requirements and this technology.

All other trademarks, registered trademarks and product names are the sole property of their respective owners.

41.5 Life Support Policy

This Chipcon product is not designed for use in life support appliances, devices, or other systems where malfunction can reasonably be expected to result in significant personal injury to the user, or as a critical component in any life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness. Chipcon AS customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Chipcon AS for any damages resulting from any improper use or sale.

42 Address Information

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Chipcon AS is an ISO 9001:2000 certified company