

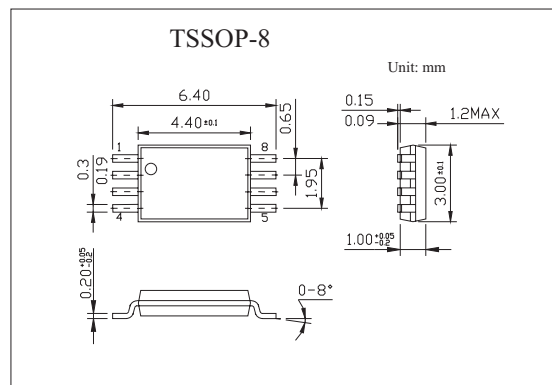
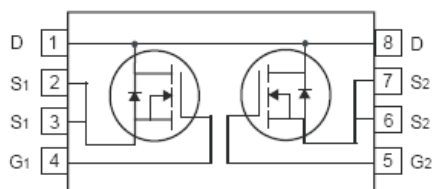


## Dual N-Channel Enhancement Mode Field Effect Transistor

### S8205A

#### ■ Features

- 5A,20V.  $r_{DS(on)} = 0.025 \Omega$  @  $V_{GS} = 4.5 V$   
 $r_{DS(on)} = 0.040 \Omega$  @  $V_{GS} = 2.5 V$ .



#### ■ Absolute Maximum Ratings $T_A = 25^\circ C$

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 8$	V
Continuous Drain Current	$I_D$	5	A
Pulsed Drain Current	$I_{DM}$	20	A
Maximum Power Dissipation $T_A = 25^\circ C$	$P_D$	2.0	W
$T_A = 70^\circ C$		1.6	W
Thermal Resistance,Junction-to-Ambient	$R_{\theta JA}$	78	$^\circ C/W$
Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	40	$^\circ C/W$
Junction temperature and Storage temperature	$T_J, T_{stg}$	-55 to +150	$^\circ C$



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## ■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V <sub>DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 $\mu$ A	20			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V			1	$\mu$ A
		V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 55°C			5	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = $\pm$ 8V			$\pm$ 50	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 $\mu$ A	0.5		1.0	V
Drain-Source On-State Resistance *	r <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 5A		0.020	0.025	$\Omega$
		V <sub>GS</sub> = 2.5V, I <sub>D</sub> = 4A		0.035	0.040	
On-State Drain Current *	I <sub>D(on)</sub>	V <sub>DS</sub> = 5V, V <sub>GS</sub> = 4.5V	15			A
Forward Transconductance *	g <sub>fs</sub>	V <sub>DS</sub> = 5V, I <sub>D</sub> = 3A		11		S
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		700		pF
Output Capacitance	C <sub>oss</sub>			175		pF
Reverse Transfer Capacitance	C <sub>rss</sub>			85		pF
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 3A		7	10	nC
Gate-Source Charge	Q <sub>gs</sub>			1.2		
Gate-Drain Charge	Q <sub>gd</sub>			1.9		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 10V I <sub>D</sub> = 1A, V <sub>GS</sub> = 4.5V, R <sub>G</sub> = 6 $\Omega$		8	16	ns
Rise Time	t <sub>r</sub>			10	18	
Turn-Off Delay Time	t <sub>d(off)</sub>			18	29	
Fall Time	t <sub>f</sub>			5	10	
Maximum Continuous Drain-Source Diode Forward Current	I <sub>S</sub>				1.3	A
Diode Forward Voltage *	V <sub>SD</sub>	I <sub>S</sub> = 1.7 A, V <sub>GS</sub> = 0 V		0.65	1.2	V

\* Pulse test; pulse width  $\leq$  300  $\mu$  s, duty cycle  $\leq$  2 %.