

NanoShield MD v1

The schematic diagram illustrates the internal circuitry of the NanoShield MD v1. It features two 15-pin headers, J1 and J2, which are connected to various components. J1 pins are labeled: 1-D1/TX, 2-D0/RX, 3, 4-D2, 5-D3, 6-DIR-A, 7-DIR-B, 8, 9-D4, 10-D5, 11-OC1A, 12-OC1B, 13-D11/HOST, 14-D12/HISO, 15. J2 pins are labeled: 1, 2, 3, 4-A7, 5-A6, 6-A5, 7-A4, 8-A3, 9-A2, 10-A1, 11, 12-A0, 13-A[7:0], 14-D13/SCK, 15. Power connections include VDD, +5V, and 3V3. The circuit includes two identical logic blocks, each containing two 74HC132D inverters (IC1A, IC1B and IC2A, IC2B), two 74HC132D NAND gates (IC1C, IC1D and IC2C, IC2D), two NPN transistors (T1A, T2A and T3A, T4A), two PNP transistors (T1B, T2B and T3B, T4B), two Schottky diodes (SL1, SL2 and SL3), and two capacitors (C1, C2). Resistors R1 through R10 are used for pull-up and pull-down. The output of the logic blocks is connected to the DIR-A and DIR-B pins of J1. The output of the logic blocks is also connected to the DIR-A and DIR-B pins of J2. The output of the logic blocks is also connected to the DIR-A and DIR-B pins of J2. The output of the logic blocks is also connected to the DIR-A and DIR-B pins of J2.

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