

LIQUID CRYSTAL DISPLAY MODULE

G 1 2 1 3 0 0 N 0 0 0

USER'S MANUAL

Seiko Instruments Inc.

This manual provides technical information covering functions and operational instructions for the G1213 liquid crystal display modules made by Seiko Instruments Inc. Please read through this manual before operating the product. Distribution of this manual to third parties for any purpose other than operation of the product is prohibited. The descriptions herein are subject to change without prior notice.

Revision Record

<u>Version</u>	<u>Revision</u>	<u>Date</u>
1	Original	December 1993

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Printed in Japan

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1. GENERAL

1.1 General

The G1213 is a very thin LCD module on which a full-dot matrix LCD panel and a CMOS IC driver are integrated. The LCD panel used here features wide viewing angle and high contrast. This full dot configuration allows a wide variety of patterns to be displayed depending upon the input data. The display position is the intersection point of the matrix transparent electrodes. This prevents display distortion and displacement. Incorporating a display RAM and a display timing signal generator into the G1213 allows for direct connection with the MPU circuit without using an LCD controller.

1.2 Features

- 128×32 full dot matrix configuration
- 1/64 duty, 1/9 bias
- A 4096-bit internal display data RAM
- An internal display timing signal generator
- 8-bit parallel interface
- Instructions:
 - Display Data Read/Write, Display ON/OFF, Display Start Line, X-Address (Page) Set, Y- Address Set, and Status Read.
- Two types of power supply: $V_{DD}=+5\text{ V}$, V_{LC}
- Reflective, gray mode
- Positive display
 - Display data "H": Display ON: blue display color
 - Display data "L": Display OFF: gray background
- A wide operating temperature range

1.3 Absolute Maximum Ratings

V_{SS} = 0 V

Item	Symbol	Conditions	Min.	Max.	Unit
Power supply voltage	V _{DD}	Ta = 25°C 50±10%RH	-0.3	7.0	V
	V _{LC}		V _{DD} -19.0	V _{DD} + 0.3	V
Input voltage	V _{IN}		-0.3	V _{DD} + 0.3	V
Operating temperature	T _{opr}	≤ 65%RH	-20	+ 70	°C
Storage temperature	T _{stg}	—	-30	+ 80	°C
Storage humidity	—	≤ 48 hrs	+20	+85	%RH
	—	≤ 1000 hrs	+20	+65	%RH

1.4 Mechanical Characteristics

Item	Standard
Dot configuration	128×32 dot
Module dimensions (H×V×T) [mm]	75.0×41.5×6.8
Viewing area (H×V) [mm]	60.0×21.3
Active display area (H×V) [mm]	55.01×16.29
Dot dimensions (H×V) [mm]	0.4×0.48
Dot pitch (H×V) [mm]	0.43×0.51
Weight [g]	27 max.

H : Horizontal V : Vertical T : Thickness (max.)

1.5 Electrical Characteristics

V_{DD} = 5V±5%, V_{SS} = 0 V, Ta = -20°C to +70°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage ¹	High	V _{IHC}	—	0.7V _{DD}	V _{DD}	V
	Low	V _{ILC}	—	0	0.3V _{DD}	V
Input voltage ²	High	V _{IHT}	—	2.0	V _{DD}	V
	Low	V _{ILT}	—	0	0.8	V
Output voltage ³	High	V _{OH}	I _{OH} = -205 μA	2.4	—	V
	Low	V _{OL}	I _{OL} = 1.6 mA	—	0.4	V
Power supply voltage	V _{DD}	—	4.75	5.00	5.25	V
	V _{LC}	—	-12.0	-8.0	-3.0	V
Current consumption ⁴	I _{DD}	V _{DD} =5 V, Ta = 25°C	—	2.0	3.0	mA
	I _{LC}	V _{LC} = -8.0 V	—	1.7	3.0	mA
Frame frequency	f _{FRM}	—	—	140	—	Hz

1 Applied to RST.

2 Applied to DB₀ to DB₇, E, R/W, D/I, CS.3 Applied to DB₀ to DB₇.

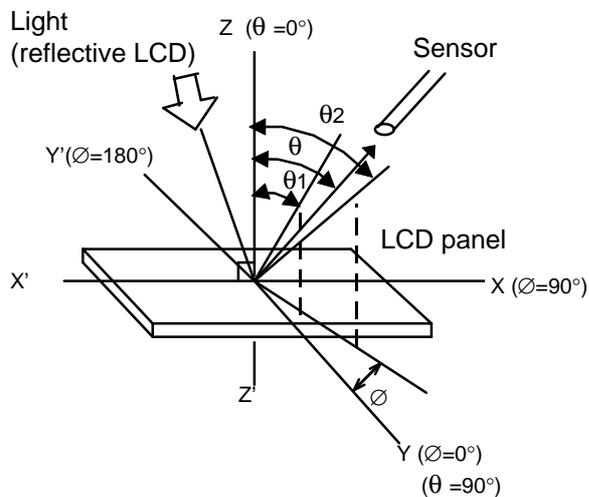
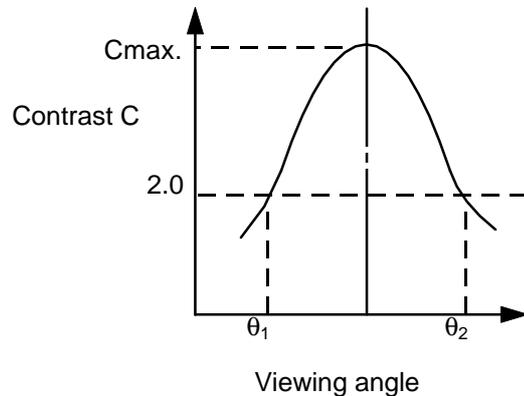
4 Display patterns: checkered patterns.

1.6 Optical Characteristics

1/64 duty, 1/9 bias, $f_{FRM} = 140 \text{ Hz}$, $V_{opr} = V_{DD} - V_{LC}$, LED backlight: OFF

Item	Sym.	Conditions	Temp.	Min.	Typ.	Max.	Unit	Remark
Viewing angle	θ_1	$C \geq 2.0$ $\varnothing = 0^\circ$ $V_{opr}=13.0 \text{ V}$	25°C	—	—	-20	Degree	Refer to notes 1 and 2
	θ_2			20	—	—		
	$\theta_2 - \theta_1$			40	—	—		
	θ_1	$C \geq 2.0$ $\varnothing = 270^\circ$ $V_{opr}=13.0 \text{ V}$	25°C	—	—	-30		
	θ_2			40	—	—		
	$\theta_2 - \theta_1$			70	—	—		
Contrast	C	$\theta = 0^\circ$ $\varnothing = 0^\circ$ $V_{opr}=13.0 \text{ V}$	25°C	4.0	6.0	—	—	Note 3
Response time	t_{on}	$\theta = 0^\circ$ $\varnothing = 0^\circ$ $V_{opr}=13.0 \text{ V}$	25°C	—	80	200	ms	Note 4
	t_{off}			—	100	200		
	t_{on}	$\theta = 0^\circ$ $\varnothing = 0^\circ$ $V_{opr}=14.4 \text{ V}$	-20°C	—	750	1200		
	t_{off}			—	1300	2000		

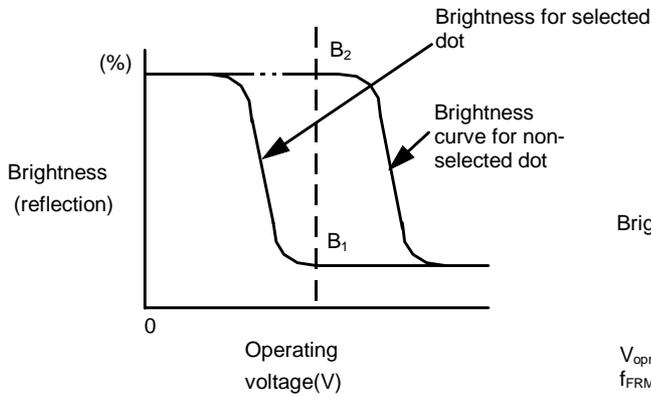
Measuring instrument : Canon illuminometer LC-3S

Note 1: Definition of angle θ and \varnothing Note 2: Definition of viewing angles θ_1 and θ_2 

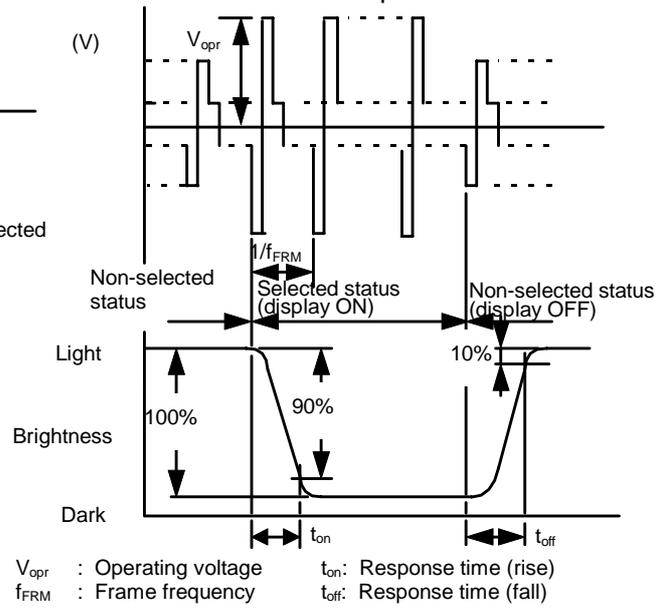
Remark: The optimum viewing angle by visual inspection and angle θ at C_{max} do not always match.

Note 3: Definition of contrast (C)

$$C = \frac{\text{Brightness of non-selected dot (reflection) } B_2}{\text{Brightness of selected dot (reflection) } B_1}$$



Note 4: Definition of response time



V_{opr} : Operating voltage t_{on} : Response time (rise)
 f_{FRM} : Frame frequency t_{off} : Response time (fall)

Note: Measurement must be made using a transmissive LCD panel.

1.7 LC panel life time

Item	Conditions	Standard	Unit
Life time ¹	25°C±10°C <65%RH	100,000 or more	hrs

1 Definition of life time: the time up to occurrence of any of the following:

- ⊘ Contrast reduces to 30% of the initial value.
- ⊘ Current consumption becomes three times the initial value.
- ⊘ Orientation deteriorates significantly.
- ⊘ The display malfunctions.

1.8 Dimensions

Unit: mm

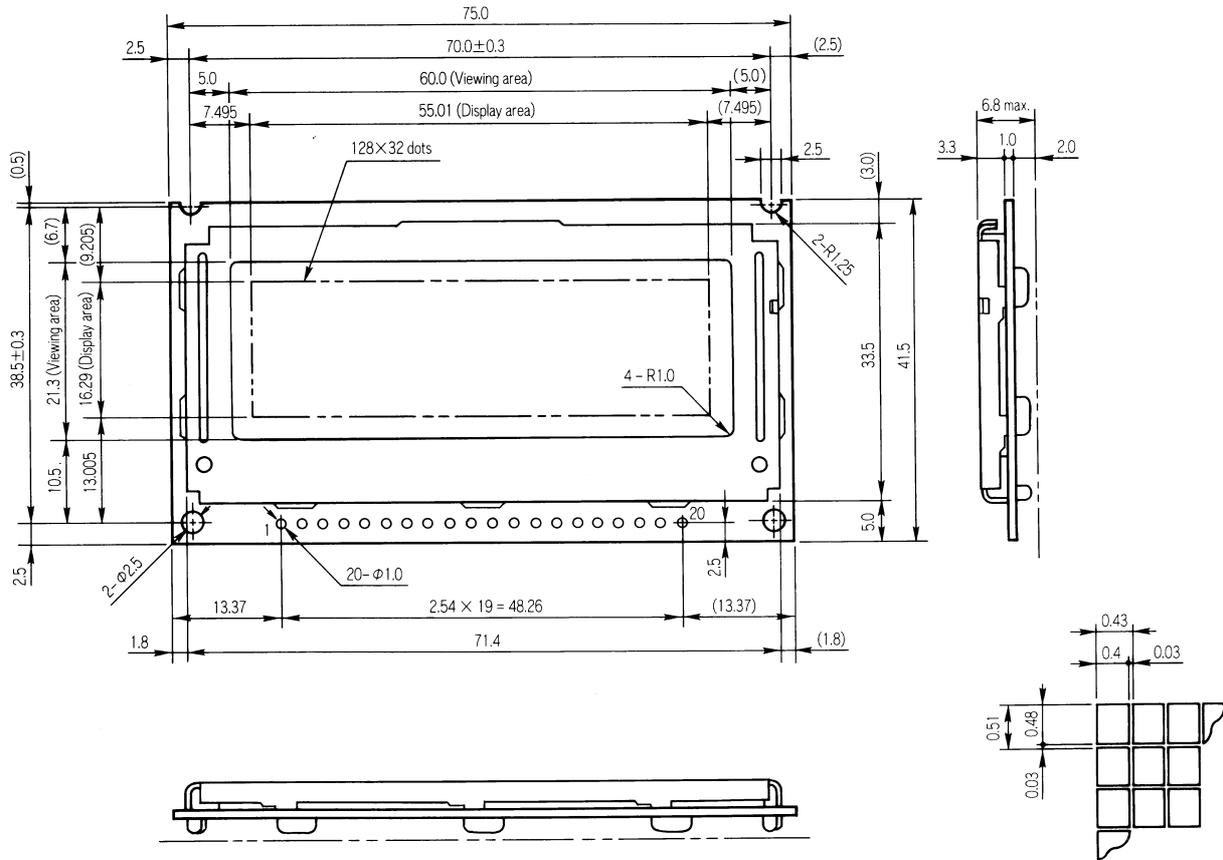
General dimensional tolerance: ± 0.5 

Figure 1 Dimensions

I/O terminal functions

No.	Sym.	Functions
1	V _{DD}	Power supply voltage: +5.0 V
2	V _{SS}	GND: 0 V
3	V _{LC}	LC drive voltage
4	DB ₀	Data bus (LSB)
5	DB ₁	Data bus
6	DB ₂	Data bus
7	DB ₃	Data bus
8	DB ₄	Data bus
9	DB ₅	Data bus
10	DB ₆	Data bus

No.	Sym.	Functions
11	DB ₇	Data bus (MSB)
12	CS	Chip select
13	RST	Reset
14	R/W	Read/Write
15	D/I	Data/Instruction
16	E	Enable
17	FGND	Frame ground ¹
18	NC	—
19	NC	—
20	NC	—

¹ FGND is connected to the metallic frame of the module. Use this frame when grounding.

2. CIRCUIT CONFIGURATION

2.1 Block Diagram

This product consists of an HD61202 segment driver, an HD61203 common driver and a bias voltage generator. Figure 2 shows the block diagram.

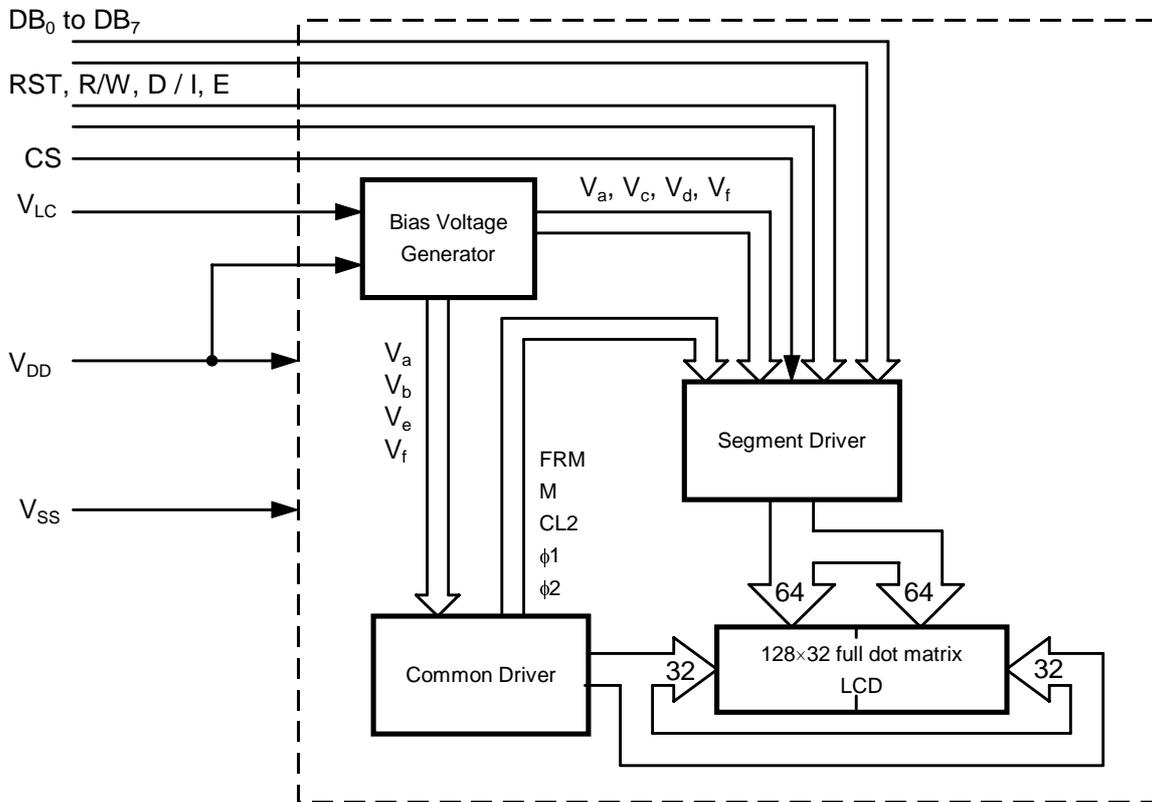


Figure 2 Block Diagram

2.2 Segment Drivers (HD61202)

The segment driver is a 64 drive output CMOS IC. A 64 (SEG1 to SEG64) \times 64 (COM1 to COM64) dot display on the segment driver is divided into a 64 (SEG1 to SEG64) \times 32 (COM1 to COM 32) dot display and a 64 (SEG1 to SEG64) \times 32 (COM33 to COM 64) dot display on the LCD display, located right and left, and is configured in a 128 \times 32 dot display. The 8 bits of data transmitted from the MPU is stored in the internal display RAM, and the segment signal is generated for LC drive. One bit of display RAM data corresponds to one dot lighting or non-lighting on the LC panel.

2.2.1 Block Diagram (Segment Driver)

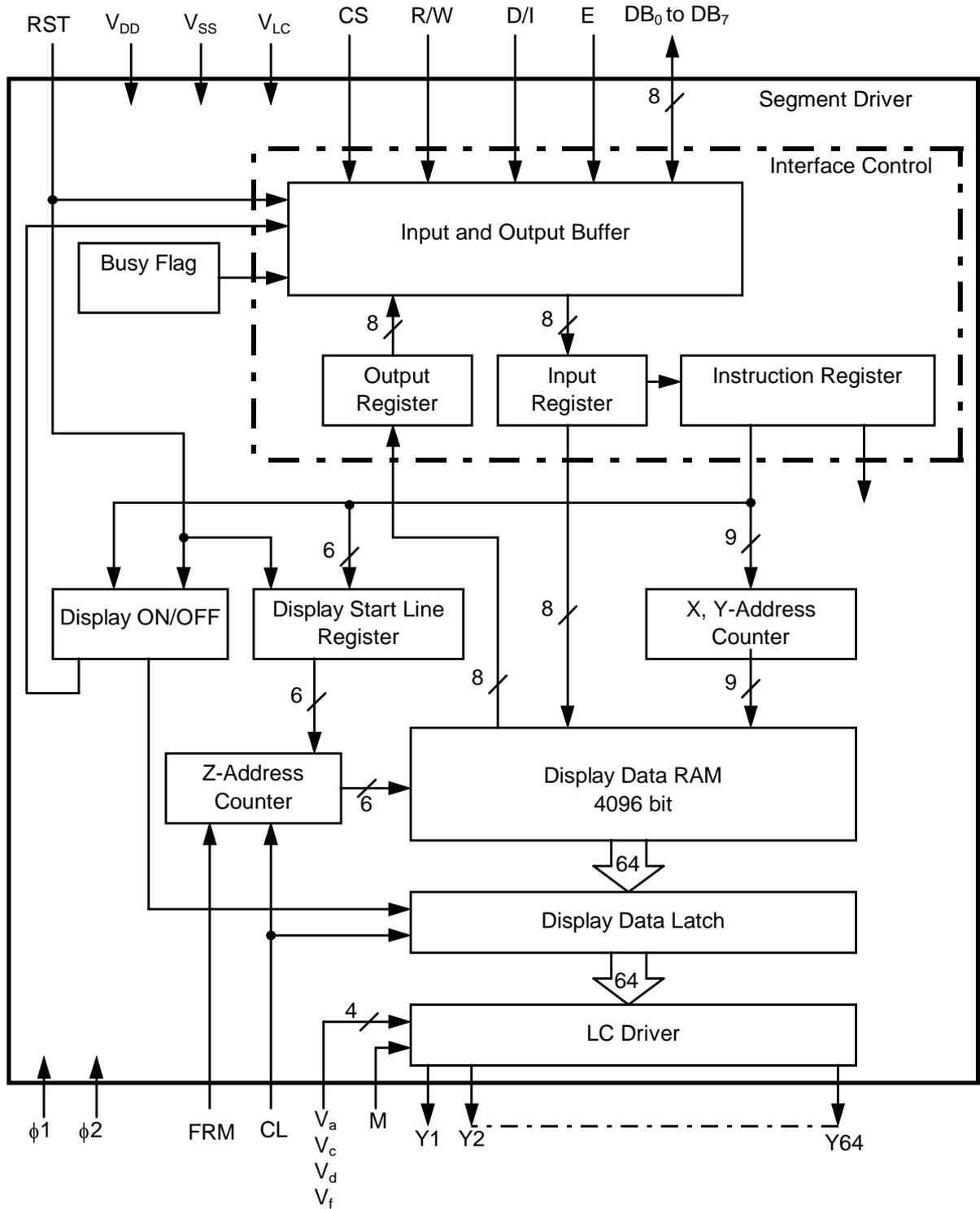


Figure 3 Segment Driver

2.2.2 Functions and Operations of Main Blocks

(1) Interface Control Unit

The interface control unit consists of the following blocks:

- ① Input and output buffer
- ② Input and output register
- ③ Instruction register

The above blocks are selected according to the following combinations of R/W and D/I signals:

D / I	R / W	Functions
1	1	Output Register Read Internal Operation (Display Data RAM → Output Register)
1	0	Input Register Write Internal Operation (Input Register → Display Data RAM)
0	1	Busy Check and Status Read
0	0	Instruction

① Input and output buffer

The data is transmitted through eight data buses (DB₀ to DB₇).

DB₇..... MSB (most significant bit)

DB₀..... LSB (least significant bit)

The data can be input and output only when the Chip Select is selected. Therefore, if the Chip Select is not selected, the internal condition remains unchanged and instruction will not be executed, even when changing the signal of the input terminals excluding the RST (reset) terminal.

Note that the RST operates regardless of CS.

② Input and output register

This product is provided with an input register and an output register so that the product can interface with MPUs having speed differing from the internal operation.

● Input register

The input register is a register that is used for temporarily storing the data to be written in the display data RAM. The data to be written from the MPU to the input register will be automatically written in the display data RAM through internal operation.

When the Chip Select is selected and R / W = 0, D / I = 0, the data is written in the register, synchronized with the fall of signal E.

● Output register

The output register is a register that is used for temporarily storing the data to be read from the display data RAM.

In order to read the content of the output register, the Chip Select must be selected, D/I must be 1, and R/W must be 1. When executing the "Read" instruction, the contents of the output register stored at that time are output during the time that "E" is 1. When "E" falls, display data of the currently indicated address is written in the output register. After that, the address advances by one.

The contents of the output register are rewritten by the Read instruction. The data is retained by the address set or other instructions. Accordingly, when performing the address set, and next executing the Read instruction, the data of the specified address is not output and the data of the address which is specified is output at the second data read time. Therefore, when setting the address, a dummy read is needed once. See Figure 4.

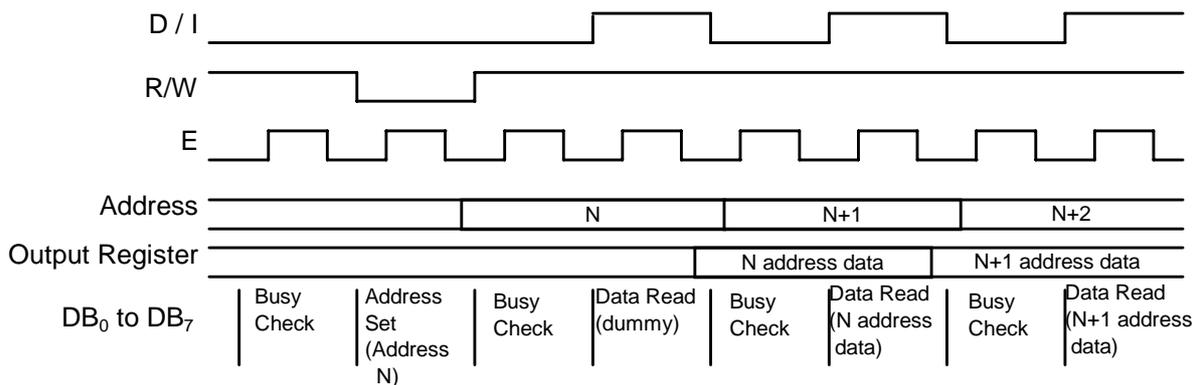
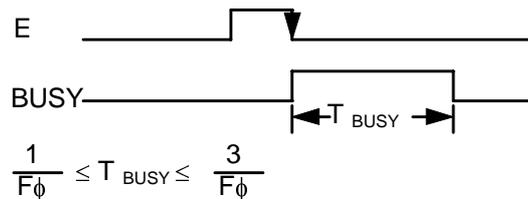


Figure 4 Read Timing

(2) Busy flag

The status when busy flag is "1" means that the module is operating internally. Instructions other than the Status Read are not available at this time. The busy flag is output to DB7 by the Status Read instruction. Ensure that the busy flag is "0" before executing the instruction.



F_φ is frequency of φ₁ or φ₂ (1 / 2 the source oscillation frequency of HD61203): 215 kHz typ.

Figure 5 Busy Flag

(3) Display ON/OFF Flip/Flop

The display ON/OFF Flip/Flop is a flip-flop function that determines whether the display data corresponding to the RAM data is output to the segment on the LCD (ON status) or goes to all nonlit status regardless of the RAM data (OFF status). This is controlled by the display ON/OFF instruction. When the RST signal becomes "0," the display goes to OFF status. This flip-flop status is output to DB5 by the Status Read instruction.

Even when performing display ON/OFF, the data inside the RAM is not affected.

(4) Display start line register

The display start line register is a register which determines the line address (see Figure 6) for which data is displayed on the top line of the left-half LCD screen when displaying the contents of the display data RAM on the LCD screen. It is also used to scroll the display. The 6 bit (0 to 63) display start line information is written in this register by the Display Start Line Set Instruction.

The contents of this register are transmitted to address counter Z at "H" level of the FRM signal (common driver output) which indicates the display start on the screen.

(5) Z-address counter

The Z-address counter generates the address to output the display data synchronized with the common signal. This is a 6-bit counter which counts at the fall of the CL signal (common driver output). The contents of the display start line register are preset to the Z-address counter at "H" level of the FRM signal (common driver output).

(6) Display data RAM

The display data RAM is a RAM that stores the display dot data. 1 bit of RAM data corresponds to lighting (data=1) or non-lighting (data = 0) of 1 dot of the display on the LCD screen. Figure 6 shows the relationship between the address and data inside the RAM on the 128×32 dot display. In this case, the display start line is 0.

Display pattern (Display start line: 0)

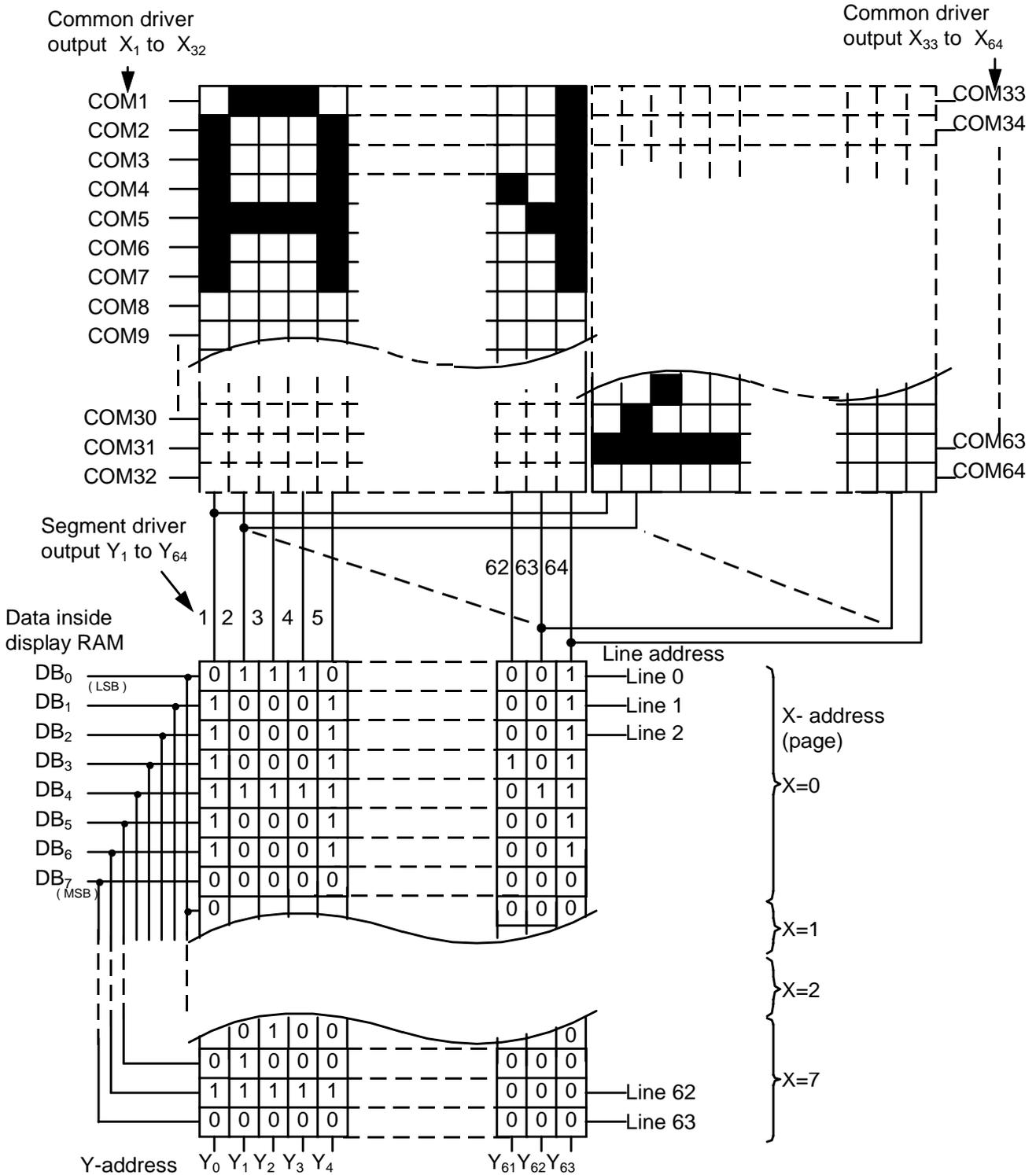


Figure 6 Relationship Between Display and Data Inside Display RAM

(7) X, Y- address counter

X, Y-address counter is a 9-bit counter which gives the address of the internal display data RAM. It is necessary to set the X-address counter of the three upper bits, and the Y-address counter of the six lower bits using differing instructions.

- X-address counter

Address counter X is a simple register that is not provided with a count function. The address is set by instruction.

- Y-address counter

This counter sets the address by instruction and is automatically advanced by the read/write operation. Counting is performed by looping the values 0 to 63.

2.3 Common driver (HD61203)

The common driver is a 64 drive output CMOS IC. Incorporating an oscillation circuit, this driver generates the common signal and timing signals (LC AC drive control, and one-frame timing signal) necessary for the LC display, and controls the display by supplying the timing signals to the segment driver.

2.4 Bias voltage generator

Six levels of standard voltage V_a to V_f are applied to the drivers as a bias voltage. This voltage is generated by resistance division of V_{opr} and driven by a voltage follower through an operational amplifier.

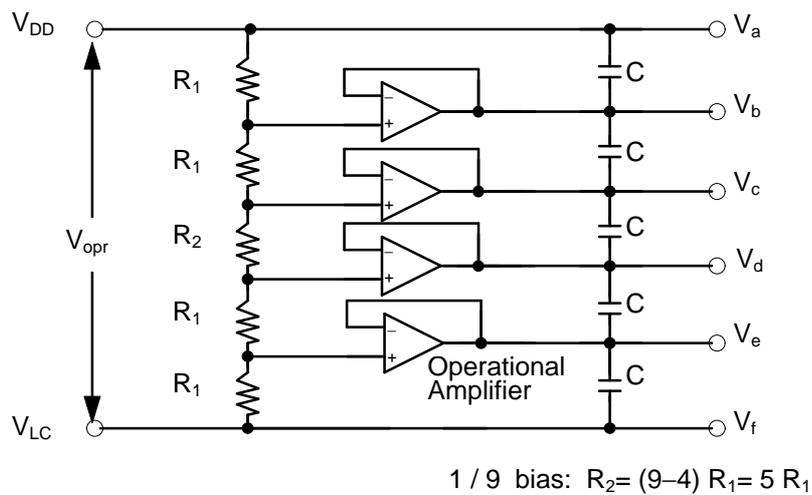


Figure 7 Bias Voltage Generator

3. OPERATING INSTRUCTIONS

3.1 Terminal Functions

Table 1 Terminal Functions

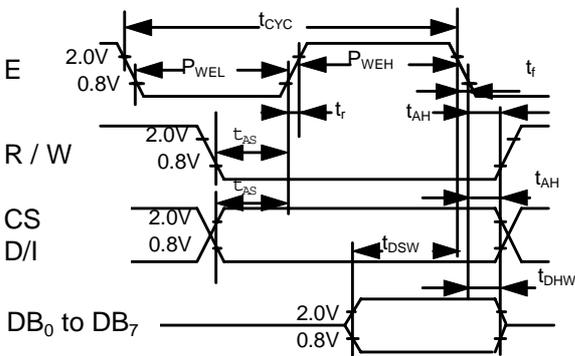
Signal	QTY	I/O	Destination	Functions				
DB ₀ to DB ₇	8	I/O	MPU	Common terminal for tristate input and output, and data bus.				
E	1	Input	MPU	Enable Write (R/W=0): Latches data of DB ₀ to DB ₇ at the fall of E. Read (R/W=1): Outputs data to DB ₀ to DB ₇ while "E" keeps a high level.				
R/W	1	Input	MPU	Read/Write selection R/W=1: When E=1 and CS=0, the data is output to DB ₀ to DB ₇ and read is available by MPU. R/W=0: When CS=0, DB ₀ to DB ₇ are ready for receiving the input.				
D/I	1	Input	MPU	Data/Instruction selection D/I=1: Indicates that the data in DB ₀ to DB ₇ is the display data. D/I=0: Indicates that the data in DB ₀ to DB ₇ is the instruction code.				
CS	1	Input	MPU	Chip select input. Data input and output is possible under the following status: <table border="1" data-bbox="730 1093 1034 1205"> <tr> <td>Terminal No.</td> <td>CS</td> </tr> <tr> <td>Status</td> <td>0</td> </tr> </table>	Terminal No.	CS	Status	0
Terminal No.	CS							
Status	0							
RST	1	Input	MPU	Reset signal Setting the RST signal to a low level allows for initial setup. (1) ON/OFF register: 0 setup (display OFF) (2) Display start line register: 0 line setup (display starts from 0 line) The setup status is retained until the status is changed by an instruction after reset is released.				
V _{DD}	1	—	Power	Power terminal for logic (+5 V)				
V _{SS}	1	—	Power	GND terminal (0 V)				
V _{LC}	1	—	Power	Power terminal for LC drive				
FGND	1	—	—	Frame ground ¹				

¹ FGND terminal is connected to the metallic frame of the module. Use this terminal when grounding the frame.

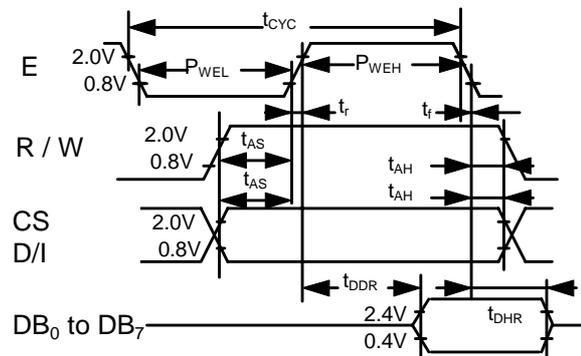
3.2 Timing Characteristics

Item	Symbol	Min.	Typ.	Max.	unit	Note
E cycle time	t_{CYC}	1000	-	-	ns	1, 2
E pulse width (H)	P_{WEH}	450	-	-	ns	1, 2
E pulse width (L)	P_{WEL}	450	-	-	ns	1, 2
E rise time	t_r	-	-	25	ns	1, 2
E fall time	t_f	-	-	25	ns	1, 2
Address setup time	t_{AS}	140	-	-	ns	1, 2
Address hold time	t_{AH}	10	-	-	ns	1, 2
Data setup time	t_{DSW}	200	-	-	ns	1
Data delay time	t_{DDR}	-	-	320	ns	2, 3
Data hold time during write	t_{DHW}	10	-	-	ns	1
Data hold time during read	t_{DHR}	20	-	-	ns	2

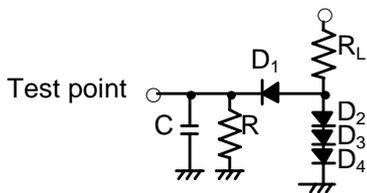
Note 1: When the MPU writes:



Note 2: When the MPU reads:



Note 3: Load circuits (DB₀ to DB₇)



$R_L = 2.4 \text{ k}\Omega$
 $R = 11 \text{ k}\Omega$
 $C = 130 \text{ pF}$ (including jig capacity)
 Diodes D1 to D4 are 1S2074 (H).

3.3 Reset Function

Setting the RST terminal to a low level when the power is on allows for initial setup.

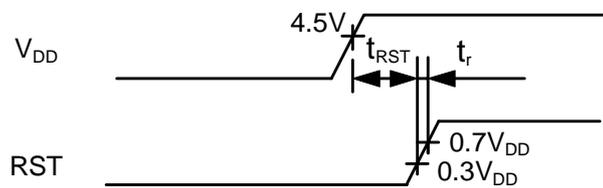
① Display OFF

② Display start line register: Set address 0.

While the RST remains at a low level, instructions other than the status read cannot be accepted. Execute other instructions after confirming that $DB_4=0$ (reset release) and $DB_7=0$ (ready), using the status read instruction.

The power conditions for power-on initial setup are as follows:.

Item	Symbol	Min	Typ.	Max	unit
Reset time	t_{RST}	1.0	—	—	μs
Rise time	t_r	—	—	200	ns



If the RESET is executed during operation, retention of the contents of all registers (excluding an ON/OFF register) and the RAM is not guaranteed. Always set them again.

3.4 Instructions

3.4.1 General

Instructions are listed on Table 2. Instructions other than the Status Read instruction will not be executed if they are sent while another instruction is already being executed. The busy flag is “1” when executing the instruction. Check whether or not the flag is “1” before transmitting the instructions from the MPU.

Table 2 List of Instructions

	Instruction	Code										Function	
		R/W	D / I	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀		
1	Display ON / OFF	0	0	0	0	1	1	1	1	1	1	1/0	Turns ON / OFF total display. Data and internal status in the display RAM remain unchanged. 1: ON 0: OFF
2	Display start line	0	0	1	1	Display start lines (0 to 63)					Determines the RAM line to be displayed on the top line (COM1) on the left-half display (SEG1 to SEG64).		
3	X-address (page) set	0	0	1	0	1	1	1	X-address(page) (0 to 7)			Sets the X -address of the RAM (page) in the X -address (page) register.	
4	Y-address set	0	0	0	1	Y-address (0 to 63)					Set Y-address of the RAM in the Y-address counter.		
5	Status read	1	0	B U S Y	0	ON / OFF	R E S E T	0	0	0	0	0	Reads the status. RESET 1: Reset 0: Normal ON/OFF 1: Display OFF 0: Display ON BUSY 1: during internal operation 0: READY status
6	Display data write	0	1	Write Data								Writes data DB ₀ (LSB) to DB ₇ (MSB) on the data bus into the display RAM.	Accesses the RAM in which address has been specified beforehand. After that the Y-address advances by one.
7	Display data read	1	1	Read Data								Reads data DB ₀ (LSB) to DB ₇ (MSB) from the display RAM into the data bus.	

Note: The BUSY time varies depending upon the frequency $F \phi$ (:215 kHz (typ.)) of $\phi 1$, $\phi 2$ ($1/F \phi \leq T_{BUSY} \leq 3/F \phi$).

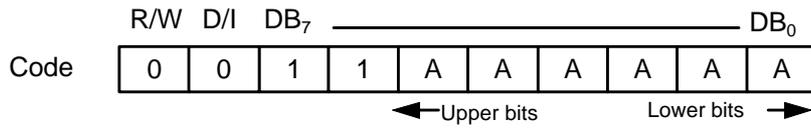
3.4.2 Detailed explanation

(1) Display ON/OFF

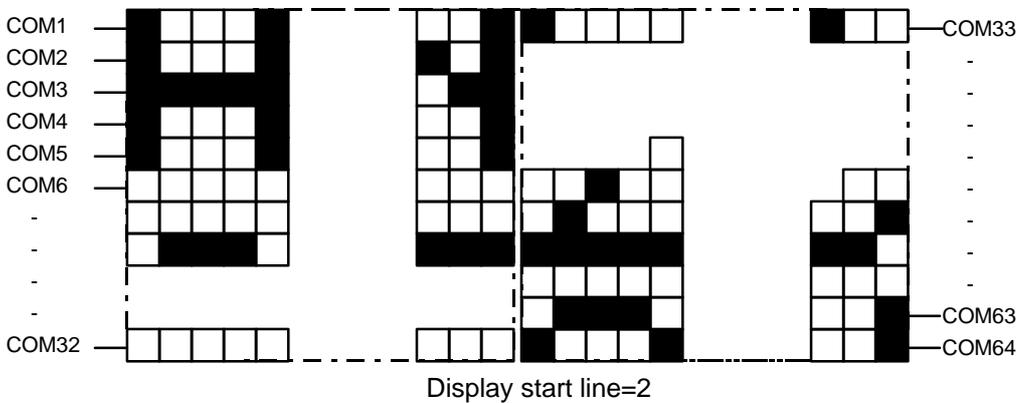
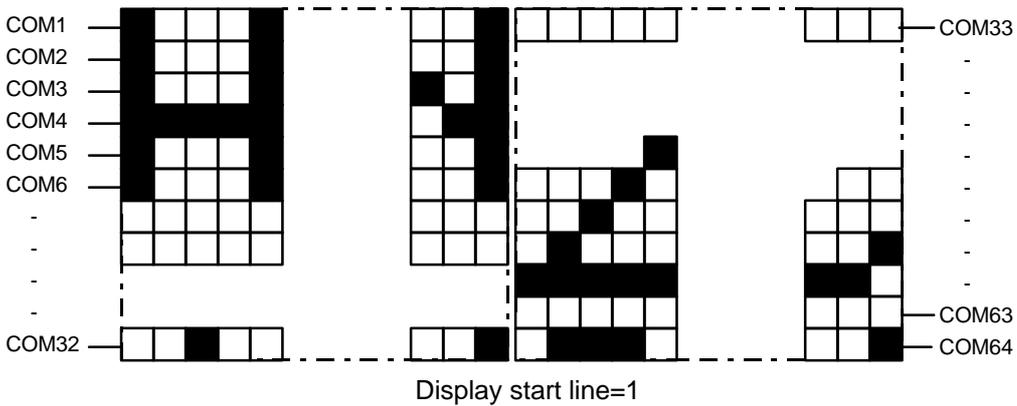
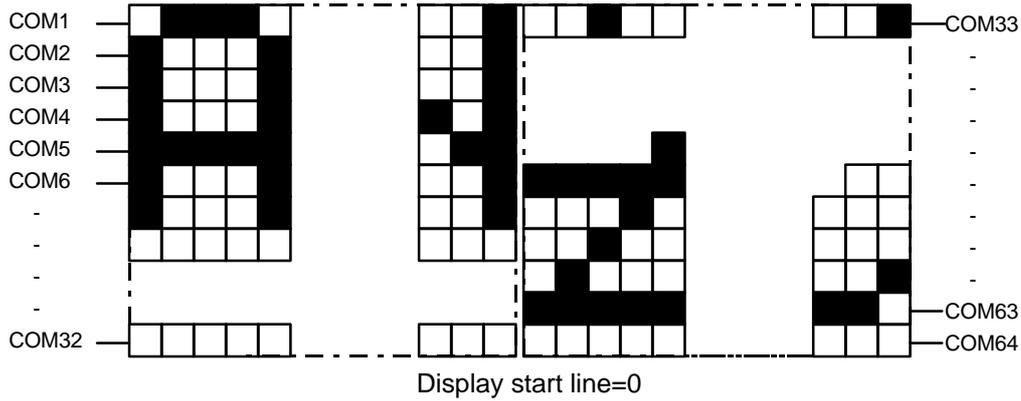
Code	R/W	D/I	DB ₇	_____	DB ₀
	0	0	0	0	1 1 1 1 1 D

Turns the display ON when D=1, and OFF when D=0. When the display is turned OFF by D=0, the original display appears if D is set to 1 because the display data is retained in the display data RAM.

(2) Display start line



Sets the display data RAM line address expressed with binary AAAAAA in the display start line register. When displaying the content of the display data RAM, the display data on the line addresses which are set in the register is displayed on the top line on the left-half LCD screen. For address configuration inside the display data, refer to Figure 6. Figure 8 shows display examples of start lines 0 to 3.



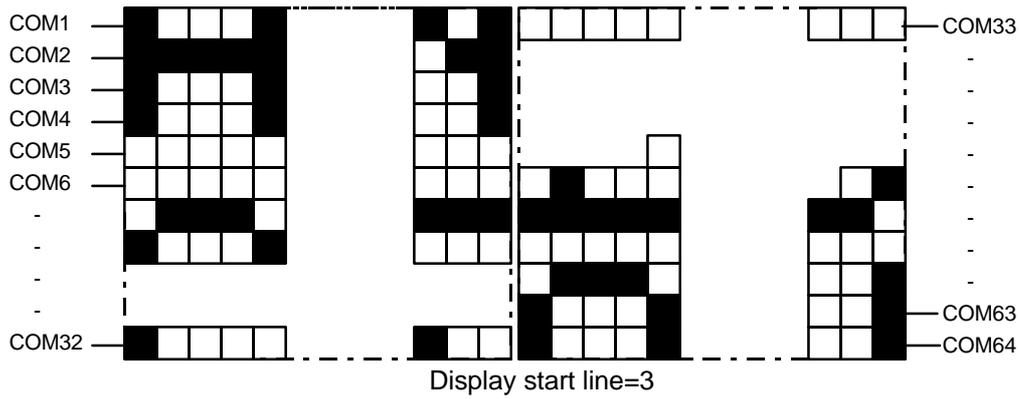
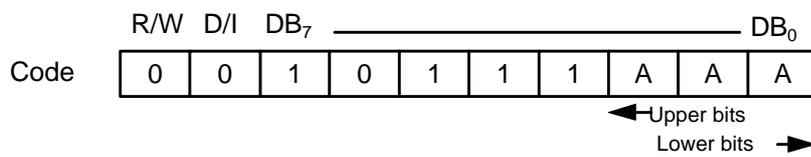


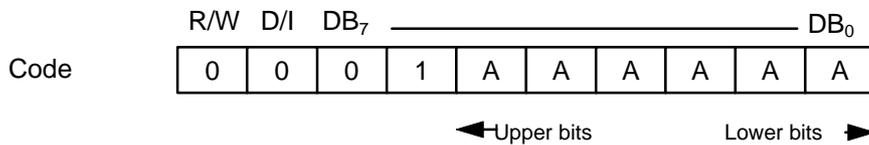
Figure 8 Relationship Between Display Start Lines and Displays

(3) X-address (page) set



The display data RAM “X” address (page) which is expressed with binary AAA is set in the X -address register. Following write/read operations from the MPU are performed on the specified X -address (page) until the next X -address (page) set is performed. The configuration of display data RAM and X -address is shown in Figure 9.

(4) Y-address set



The display data RAM Y- address which is expressed with binary AAAAAA is set in the Y-address counter. After that the Y-address counter advances by one each time write/read is performed from the MPU. The configuration of the display data RAM and Y-address is shown in Figure 9.

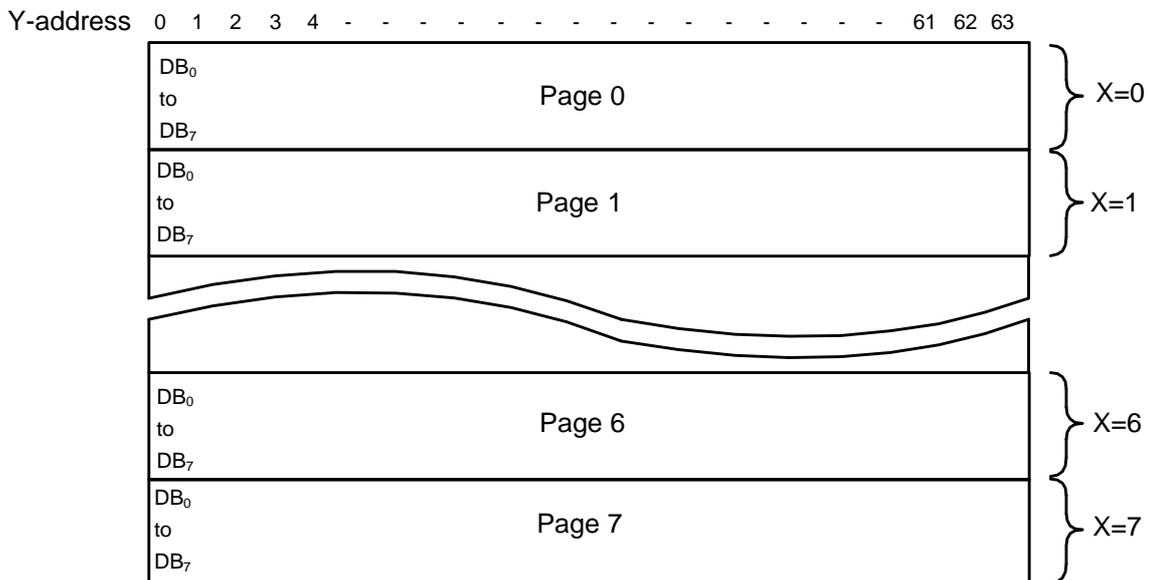
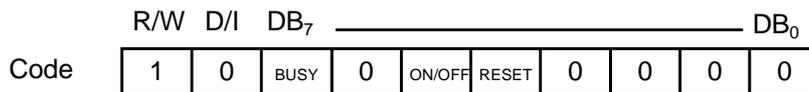


Figure 9 Display Data RAM Address Configuration

(5) Status read

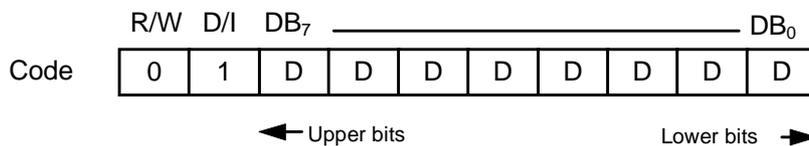


BUSY: When BUSY=1, it means that the the module is operating internally and the next instruction is not accepted until BUSY=0. After confirming that BUSY=0, it is necessary to perform the next write.

ON/OFF: Indicates that the display is OFF when ON/OFF=1.
Indicates that the display is ON when ON/OFF=0.

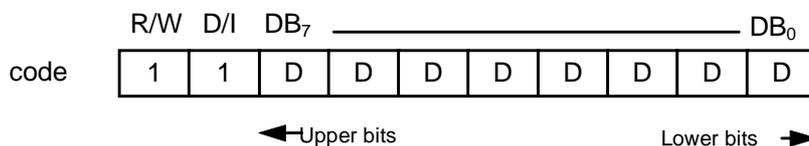
RESET: Indicates that initial setup is performed by the RST signal.
Indicates that the initialization is being performed when RESET=1 and instructions other than the Status Read instruction are not accepted.
When RESET=0, initialization is completed and operation status is normal.

(6) Display data write



Writes 8-bit binary data DDDDDDDD in the display data RAM. After the write is completed, the Y-address is automatically advanced by one

(7) Display data read



Read 8-bit binary data DDDDDDDD from the display data RAM. After read is performed, the Y-address is automatically advanced by one. A dummy read is necessary once, immediately after the address set is completed. For details, refer to segment driver output register section.

3.5 Contrast Adjustment and Power Supply Example

The LC panel viewing angle and display screen contrast are greatly affected by the ambient temperature. The recommended LC drive voltage (V_{opr}) at each temperature is given below. V_{opr} is a value at which the best display is visually obtained. This value does not always correspond to the value at which the best contrast ($C_{max.}$) is obtained. A contrast adjustment circuit example is shown below:

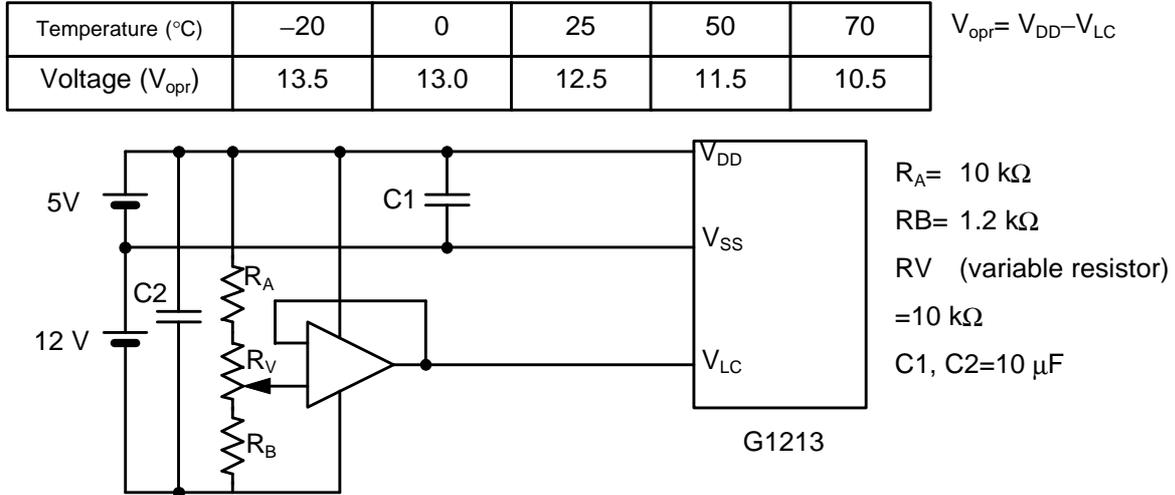


Figure 10 Contrast Adjustment

3.6 MPU Connection Diagram

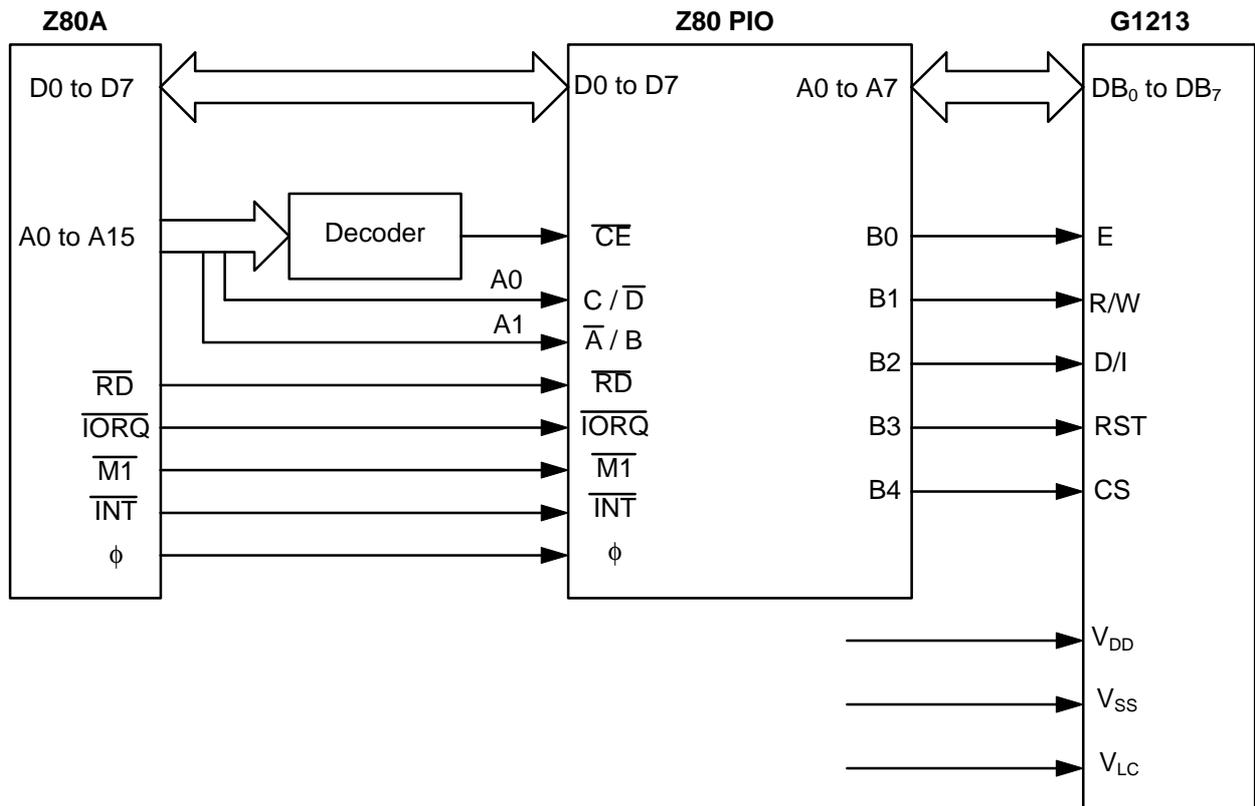


Figure 11 Example of Connection to Z80A

4. PRECAUTIONS

Safety

- If the LCD panel is damaged, be careful not to get the liquid crystal in your mouth. If the liquid crystal touches your skin or clothes, promptly wash it off using soap and plenty of water.

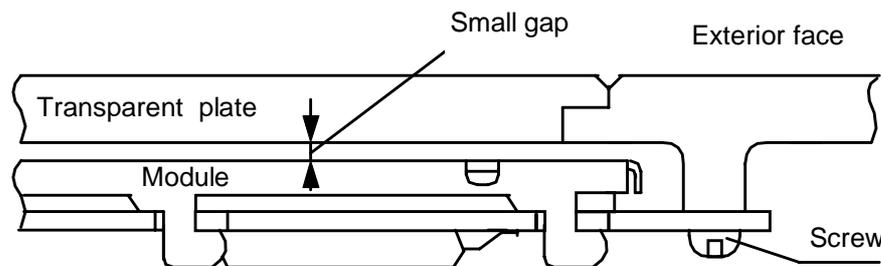
Handling

- Avoid static electricity, as it will damage the CMOS LSI.
- The LCD panel is made of plate glass. Do not hit or crush it.
- Do not remove the panel or frame from the module.
- The polarizer of the display is very fragile. Handle it very carefully.

Mounting and design

- Mount the module by using the specified mounting parts and holes.
- To protect the module against external pressure, place a transparent plate (e.g., acrylic or glass) on the module, leaving a small gap between the display surface and transparent plate.

☆Example



- Design the system so that no input signal is given unless the power-supply voltage is applied.
- Keep the module dry. Avoid condensation to prevent the transparent electrodes from being damaged.

Storage

- Store the module in a dark place, where the temperature is $25^{\circ}\text{C} \pm 10^{\circ}\text{C}$ and the relative humidity below 65%.
- Do not store the module near organic solvents or corrosive gases.
- Keep the module (including accessories) safe from vibration, shock and external pressure.

Cleaning

- Do not wipe the polarizer with a dry cloth, as it may scratch the surface.
- Wipe the module gently with a soft cloth soaked with a petroleum benzine.
- Do not use ketonic (ketone) solvents (ketone and acetone) or aromatic solvents (toluene and xylene), as they may damage the polarizer.

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