Advanced Information
Preliminary Datasheet

OV9660 Color CMOS SXGA (1.3 MegaPixel) CAMERACHIP™ Sensor with OmniPixel2™ Technology

General Description

The OV9660 CAMERACHIP™ image sensor is a low voltage CMOS device that provides the full functionality of a single-chip SXGA (1280x1024) camera and image processor in a small footprint package. The OV9660 provides full-frame, sub-sampled, scaled or windowed 8-bit/10-bit images in a wide range of formats, controlled through the Serial Camera Control Bus (SCCB) interface.

This product has an image array capable of operating at up to 15 frames per second (fps) in SXGA resolution with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control, defect pixel canceling, noise canceling, and more, are also programmable through the SCCB interface. In addition, OmniVision sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable color image.

Note: The OV9660 uses a lead-free package.

Features

- High sensitivity for low-light operation
- Low operating voltage for embedded portable applications
- Standard SCCB interface
- Supports image sizes: SXGA, VGA, CIF, scaled down and windowed outputs with Raw RGB, RGB565/555/444, YUV (4:2:2) and YCbCr (4:2:2) formats
- VarioPixel® method for sub-sampling
- Automatic image control functions including Automatic Exposure Control (AEC), Automatic Gain Control (AGC), Automatic White Balance (AWB), and Automatic Black-Level Calibration (ABLC)
- Image quality controls including color saturation, hue, gamma, sharpness (edge enhancement), lens correction, defect pixel canceling, noise canceling, and 50/60 Hz luminance detection

Ordering Information

Product	Package
OV09660-VL9A (Color, lead-free)	26-pin CSP2

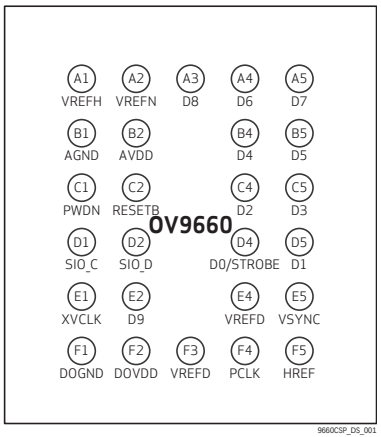
Applications

- Cellular and Picture Phones
- Toys
- PC Multimedia
- Digital Still Cameras

Key Specifications

	Active Array Size	1304 x 1036
Power Supply	**Analog**	2.45 to 3.0VDC
	I/O	1.71V to 3.0V
Power Requirements	**Active**	80 mW typical (15fps)
	Standby	15 µA typical
Temperature Range	**Operation**	-30°C to 70°C
	Stable Image	0°C to 50°C
Output Formats (8-bit)		• YUV/YCbCr 4:2:2 • RGB565/555/444 • Raw RGB Data
	Lens Size	1/5.5"
	Chief Ray Angle	25° non-linear
Maximum Image Transfer Rate	**SXGA**	15 fps
	VGA and down scaling	30 fps
	Sensitivity	450 mV/(Lux • sec)
	S/N Ratio	40 dB
	Dynamic Range	55 dB
	Scan Mode	Progressive
	Maximum Exposure Interval	1052 x t_{ROW}
	Gamma Correction	Programmable
	Pixel Size	2.0 µm x 2.0 µm
	Dark Current	3 mV/sec @ 60°C
	Well Capacity	13 Ke
	Fixed Pattern Noise	1% of $V_{PEAK-TO-PEAK}$
	Image Area	2608 µm x 2072 µm
	Package Dimensions	4485 µm x 4985 µm

Figure 1 OV9660 Pin Diagram (Top View)[1]



[1] OV9660 pin diagram © 2007 OmniVision Technologies, Inc.

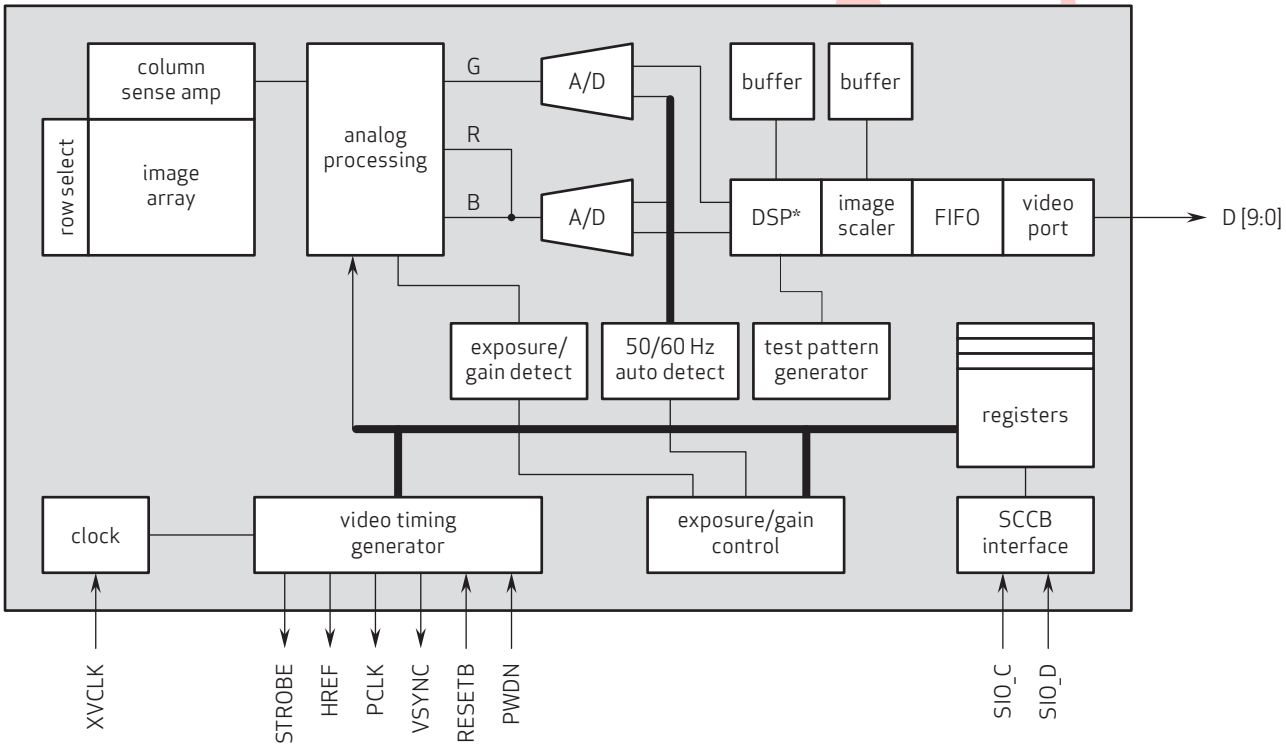
Version 1.6, April 5, 2007

Functional Description

Figure 2 shows the functional block diagram of the OV9660 image sensor. The OV9660 includes:

- Image Sensor Array (1304 x 1036 active image array)
- Analog Signal Processor
- A/D Converters
- Digital Signal Processor (DSP)
- Output Formatter
- Timing Generator
- SCCB Interface
- Digital Video Port

Figure 2 Functional Block Diagram



note 1 DSP* (lens shading correction, de-noise, defect pixel correction, auto white balance, etc.)

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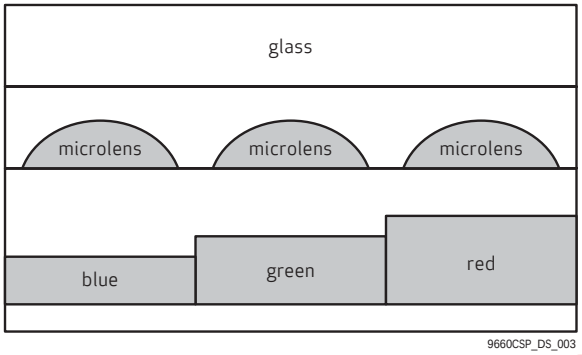
Image Sensor Array

The OV9660 sensor has an active image array of 1304 columns by 1036 rows (1,350,944 pixels). Figure 3 shows a cross-section of the image sensor array.

Figure 3 Image Sensor Array



Timing Generator

In general, the timing generator controls the following functions:

- Array control and frame generation
- Internal timing signal generation and distribution
- Frame rate timing
- Automatic Exposure Control (AEC)
- External timing outputs (VSYNC, HREF/HSYNC, and PCLK)

Analog Signal Processor

This block performs Automatic Gain Control (AGC).

A/D Converters

After the Analog Processing block, the bayer pattern Raw signal is fed to two 10-bit analog-to-digital (A/D) converters, one for the G channel and one shared by the BR channels. These A/D converters operate at speeds up to 27 MHz and are fully synchronous to the pixel rate (actual conversion rate is related to the frame rate).

In addition to the A/D conversion, this block also has the following functions:

- Digital Black-Level Calibration (BLC)
- Optional U/V channel delay
- Additional A/D range controls

In general, the combination of the A/D Range Multiplier and A/D Range Control sets the A/D range and maximum value to allow the user to adjust the final image brightness as a function of the individual application.

Digital Signal Processor (DSP)

This block controls the interpolation from Raw data to RGB and some image quality control.

- Automatic White Balance (AWB)
- Edge enhancement (a two-dimensional high pass filter)
- Color space converter (can change Raw data to RGB or YUV/YCbCr)
- RGB matrix to eliminate color cross talk
- Hue and saturation control
- Programmable gamma control
- Transfer 10-bit data to 8-bit
- Defect pixel canceling
- De-noise

Output Formatter

This block controls all output and data formatting required prior to sending the image out.

Strobe Mode

The OV9660 has a Strobe mode that allows it to work with an external flash and LED.

Digital Video Port

Register bits COM2[1:0] increase I_{OL}/I_{OH} drive current and can be adjusted as a function of the customer's loading.

SCCB Interface

The Serial Camera Control Bus (SCCB) interface controls the CAMERACHIP sensor operation. Refer to *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

Pin Description[1]

Table 1 Pin Description

Pin Location	Name	Pin Type	Function/Description
A1	VREFH	Reference	Internal analog voltage reference - connect to analog ground through a 0.1µF capacitor
A2	VREFN	Reference	Internal analog voltage reference - connect to analog ground through a 0.1µF capacitor
A3	D8	Output	Video output bit[8]
A4	D6	Output	Video output bit[6]
A5	D7	Output	Video output bit[7]
B1	AGND	Power	Ground for analog circuit
B2	AVDD	Power	Power for analog circuit
B4	D4	Output	Video output bit[4]
B5	D5	Output	Video output bit[5]
C1	PWDN	Input	Power down function (active high) with internal pull-down resistor
C2	RESETB	Input	Reset function (active low) with internal pull-up resistor
C4	D2	Output	Video output bit[2]
C5	D3	Output	Video output bit[3]
D1	SIO_C	Input	SCCB serial interface clock input without internal pull-up/pull-down resistor
D2	SIO_D	I/O	SCCB serial interface data I/O
D4	D0/STROBE	Output	Video output bit[0] when in 10-bit output mode or Strobe output when in 8-bit output mode.
D5	D1	Output	Video output bit[1]
E1	XVCLK	Input	System clock input without internal pull-up/pull-down resistor
E2	D9	Output	Video output bit[9]
E4	VREFD	Reference	Digital reference - connect to digital ground through a 0.1µF capacitor and connect with pin F3
E5	VSYNC	Output	Vertical sync output
F1	DOGND	Power	Ground for digital / video port
F2	DOVDD	Power	Power for digital / video port
F3	VREFD	Reference	Digital reference - connect to digital ground through a 0.1µF capacitor and connect to pin E4
F4	PCLK	Output	Pixel clock output
F5	HREF	Output	Horizontal reference output

NOTE:
D[9:2] for 8-bit YUV or RGB565/RGB555 (D[9] MSB, D[2] LSB)
D[9:0] for 10-bit Raw RGB data (D[9] MSB, D[0] LSB)

[1] OV9660 pin description list © 2007 OmniVision Technologies, Inc.

Electrical Characteristics

Table 2 Absolute Maximum Ratings

Ambient Storage Temperature		-40ºC to +95ºC
Supply Voltages (with respect to Ground)	**V_{DD-A}**	4.5 V
	V_{DD-IO}	4.5 V
All Input/Output Voltages (with respect to Ground)		-0.3V to V_{DD-IO}+0.5V
Lead-free Temperature, Surface-mount process		245ºC

NOTE: Exceeding the Absolute Maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent device damage.

Table 3 DC Characteristics (-30°C < T_A < 70°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD-A}	DC supply voltage – analog	–	2.45	2.8	3.0	V
V_{DD-IO}	DC supply voltage – I/O	–	1.71	1.8	3.0	V
I_{DDA}	Active (operating) current	See Note [a]		17 + 18[b]	50	mA
$I_{DDS-SCCB}$	Standby current	See Note [c]		1	2	mA
$I_{DDS-PWDN}$	Standby current			15	30	µA
V_{IH}	Input voltage HIGH	CMOS	0.7 x V_{DD-IO}			V
V_{IL}	Input voltage LOW				0.3 x V_{DD-IO}	V
V_{OH}	Output voltage HIGH	CMOS	0.9 x V_{DD-IO}			V
V_{OL}	Output voltage LOW				0.1 x V_{DD-IO}	V

a. At 25°C, V_{DD-A} = 2.8V, V_{DD-IO} = 1.8V
$I_{DDA} = \Sigma\{I_{DD-A} + I_{DD-IO}\}$, f_{CLK} = 24MHz at 15 fps YCbCr output with typical loading

b. I_{DD-IO} = 17mA, I_{DD-A} = 18mA, with typical loading

c. At 25°C, V_{DD-A} = 2.8V, V_{DD-IO} = 1.8V
$I_{DDS-SCCB}$ refers to a SCCB-initiated Standby, while $I_{DDS-PWDN}$ refers to a PWDN pin-initiated Standby

Table 4 Functional and AC Characteristics (-30°C < T_A < 70°C)

Symbol	Parameter		Min	Typ	Max	Unit
Functional Characteristics						
	A/D Differential non-linearity			± 1/2		LSB
	A/D Integral non-linearity			± 1		LSB
Inputs (PWDN, XVCLK and RESETB)						
f_{CLK}	Input clock frequency	With PLL	10	24	27	MHz
		Without PLL	10	24	54	MHz
$t_{CLK:DC}$	Clock duty cycle		45	50	55	%
$t_{S:RESETB}$	Setting time after software/hardware reset				1	ms
$t_{S:REG}$	Settling time for register change				300	ms
SCCB Timing (see Figure 4)						
f_{SIO_C}	Clock frequency				400	KHz
t_{LOW}	Clock low period		1.3			µs
t_{HIGH}	Clock high period		600			ns
t_{AA}	SIO_C low to data out valid		100		900	ns
t_{BUF}	Bus free time before new START		1.3			µs
$t_{HD:STA}$	START condition hold time		600			ns
$t_{SU:STA}$	START condition setup time		600			ns
$t_{HD:DAT}$	Data in hold time		0			µs
$t_{SU:DAT}$	Data in setup time		100			ns
$t_{SU:STO}$	STOP condition setup time		600			ns
t_{R}, t_{F}	SCCB rise/fall times				300	ns
t_{DH}	Data out hold time		50			ns
Outputs (VSYNC, HREF, PCLK, and D[9:0] (see Figure 5, Figure 6, and Figure 7)						
t_{PDV}	PCLK[↓] to data out valid				5	ns
t_{SU}	D[9:0] setup time		15			ns
t_{HD}	D[9:0] hold time		8			ns
t_{PHH}	PCLK[↓] to HREF[↑]		0		5	ns
t_{PHL}	PCLK[↓] to HREF[↓]		0		5	ns
AC Conditions:	• V_{DD}: V_{DD-A} = 2.8V, V_{DD-IO} = 1.8V • Rise/Fall Times: I/O: 5ns, Maximum SCCB: 300ns, Maximum • Input Capacitance: 10pf • Output Loading: 20pF • f_{CLK}: 24MHz					

Timing Specifications

Note: Timing may vary depending on register settings.

Figure 4 SCCB Timing Diagram

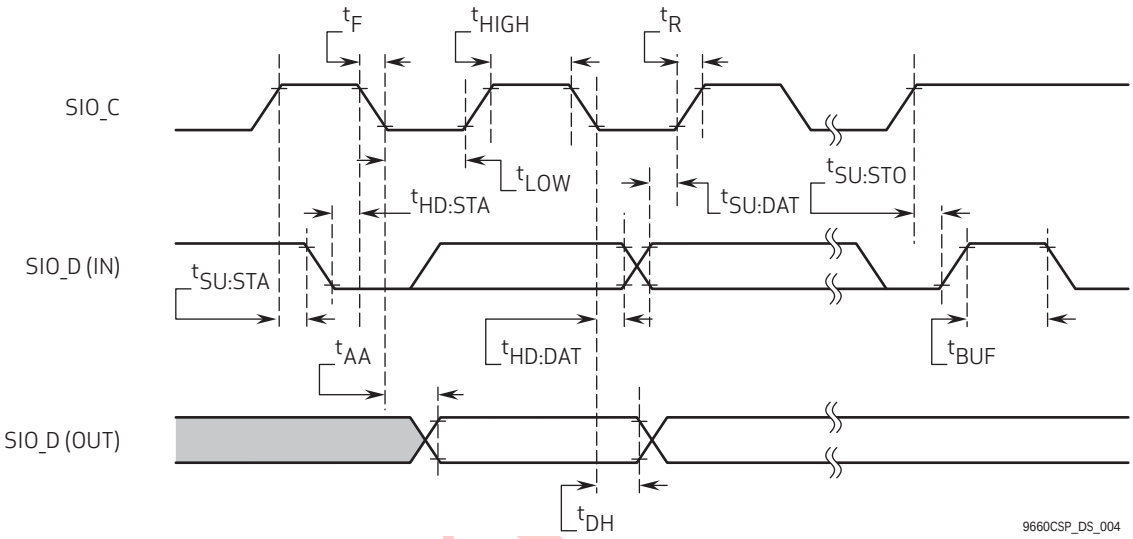


Figure 5 Horizontal Timing

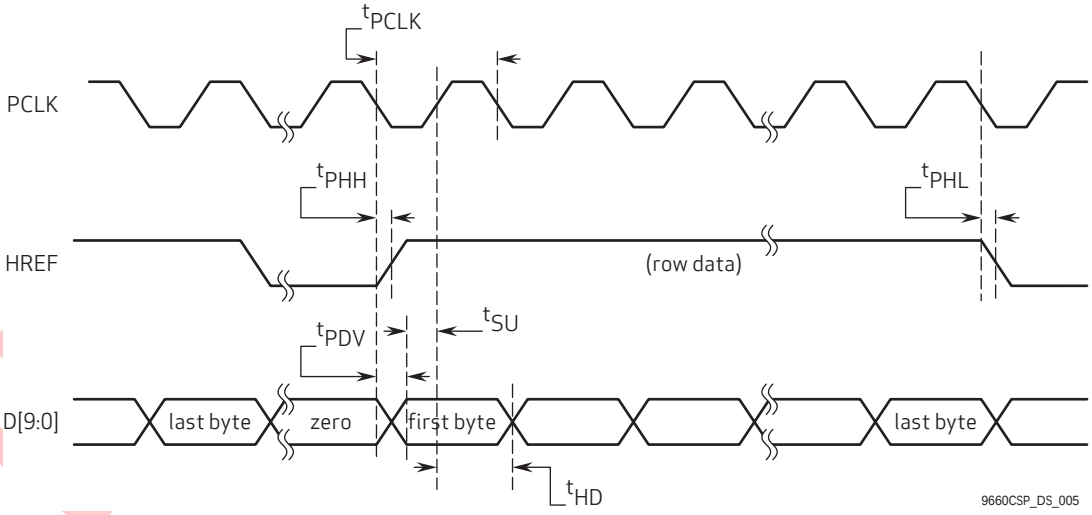
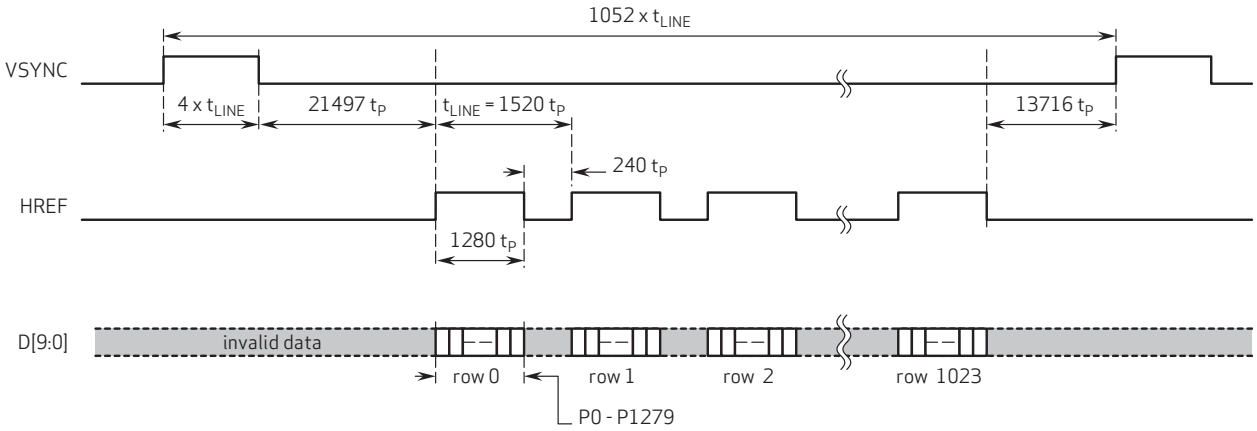


Figure 6 SXGA Frame Timing



note1 for raw data, t_P = internal pixel clock

note2 for YUV/RGB, t_P = 2 x internal pixel clock

note3 this timing diagram is for reference only; different settings will result in different timing values

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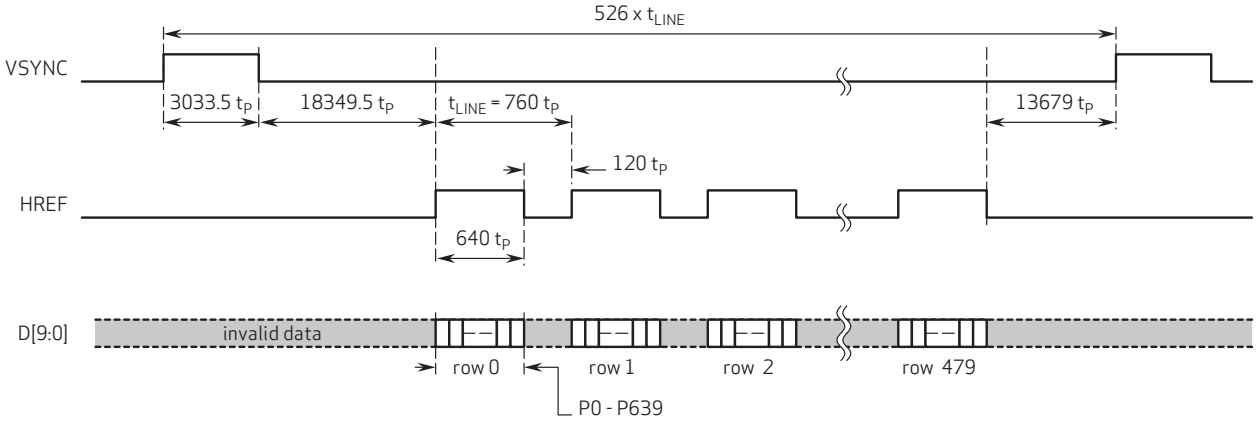
Figure 7 VGA 30 Frame Timing



note1 for raw data, t_P = internal pixel clock

note2 for YUV/RGB, t_P = 2 x internal pixel clock

note3 this timing diagram is for reference only; different settings will result in different timing values

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Figure 8 RGB 565 Output Timing Diagram

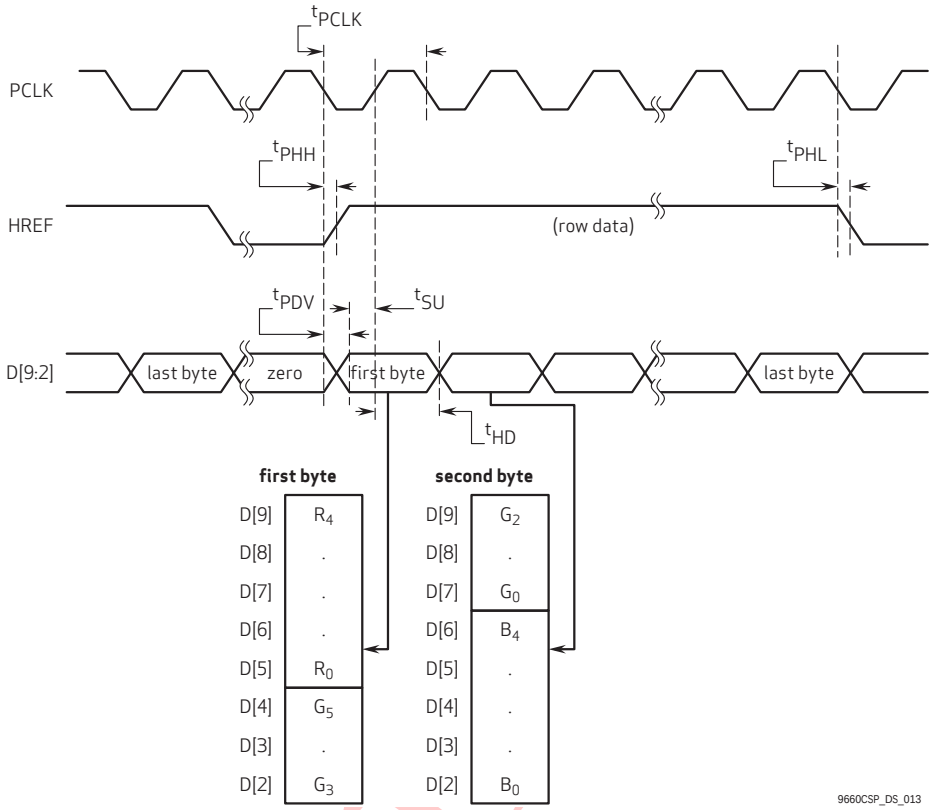


Figure 9 RGB 555 Output Timing Diagram

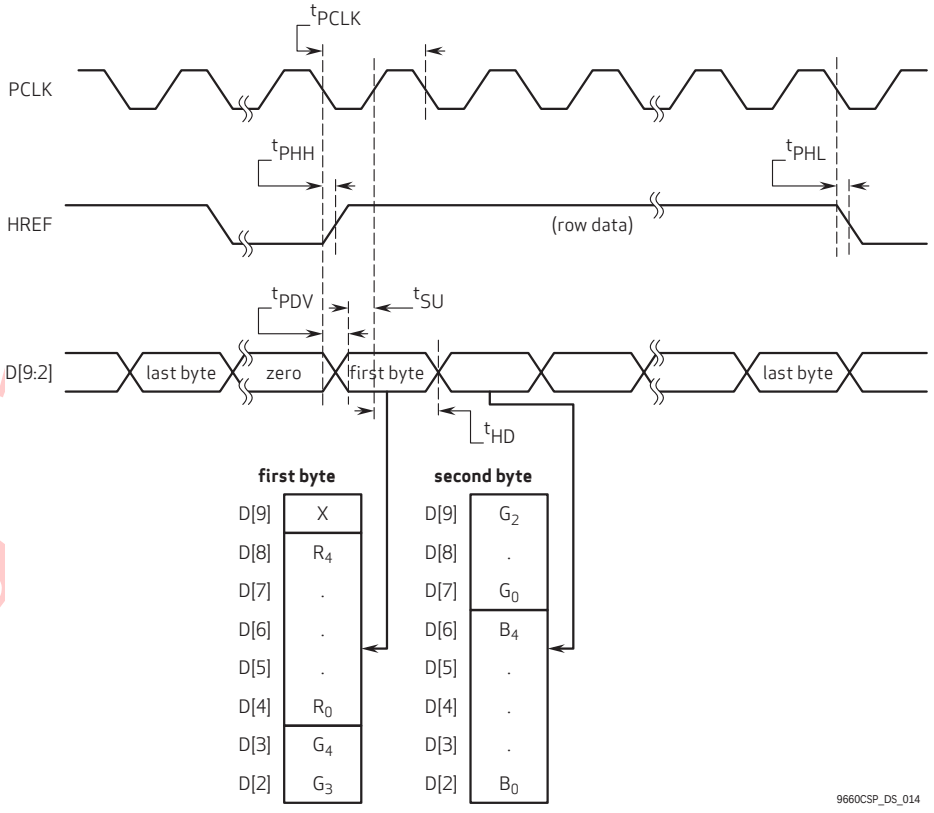
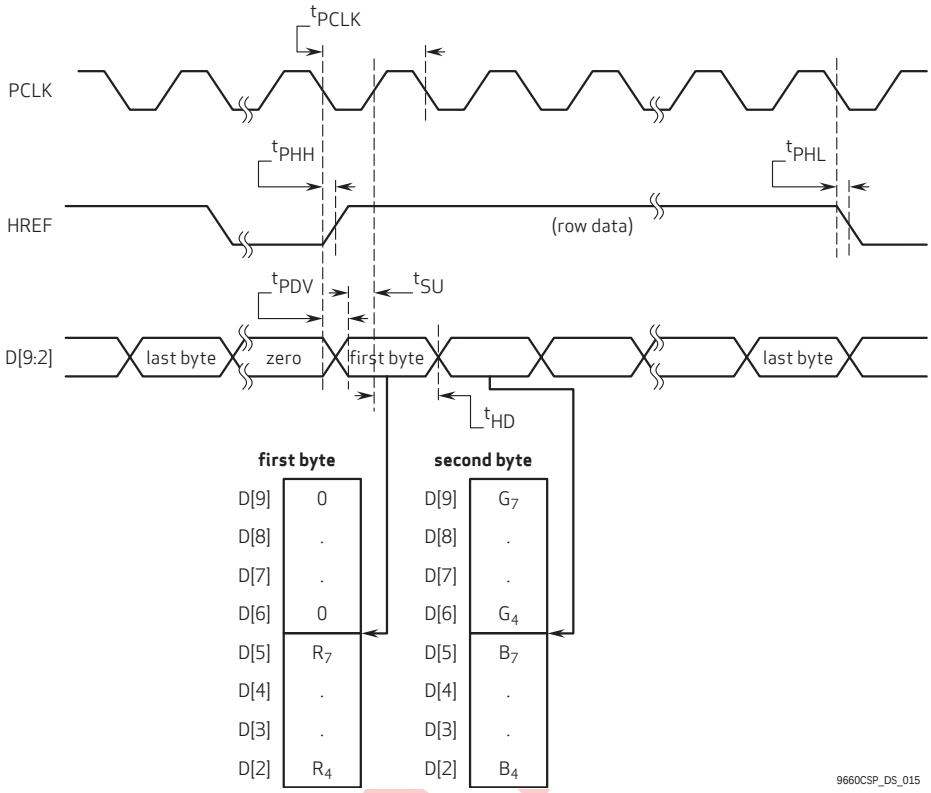


Figure 10 RGB 444 Output Timing Diagram



Register Table

Table 5 provides a list and description of the Device Control registers contained in the OV9660. For all register Enable/Disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0x60 for write and 0x61 for read.

Note: Reserved registers or register bits may be non-functional, special function or sensitive to the sensor. Please refer to OmniVision's recommended register settings.

Table 5 Device Control Register List (Sheet 1 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC Gain Control Bit[7:0]: Gain setting • Range: 1x to 32x Gain = (Bit[7]+1) x (Bit[6]+1) x (Bit[5]+1) x (Bit[4]+1) x (1+Bit[3:0])/16) ***NOTE**: Set COM8[2] = 0 to disable AGC.*
01	BLUE	40	RW	Blue Gain Control
02	RED	40	RW	Blue Gain Control
03	COM1	03	RW	Common Control 1 Bit[7:6]: Dummy frame control - effective when register bit COM6[3] = 1 (0x0F) (night mode enable) 00: Not used 01: Allow 1 dummy frame 10: Allow 3 dummy frames 11: Allow 7 dummy frames Bit[5:4]: Reserved Bit[3:2]: Vertical window end line control 2 LSBs (see register VEND for 8 MSBs) Bit[1:0]: Vertical window start line control 2 LSBs (see register VSTRT for 8 MSBs)
04	REG04	28	RW	Register 04 Bit[7]: Horizontal mirror (effective when register bit REG33[3] = 1 (0x33) Bit[6]: Vertical flip Bit[5:2]: Reserved Bit[1:0]: AEC low 2 LSBs – AEC[1:0] (see register AEC for AEC[9:2] and register REG45[5:0] for AEC[15:10])
05	REG05	00	RW	Register 05 Bit[7:3]: Reserved Bit[2:0]: UV adjust slope[5:3] between gain threshold 1 and gain threshold 2. For others, refer to registers COM1[5:4] (0x03) and REG60[2:0] (0x60).

Table 5 Device Control Register List (Sheet 2 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
06	REG06	10	RW	Register 06 Bit[7:6]: Dummy line insertion beginning gain 00: 2x 01: 4x 10: 8x 11: 8x Bit[5:0]: Reserved
07	REG07	24	RW	Register 07 Bit[7]: Reserved Bit[6:4]: VS start point Bit[3]: Reserved Bit[2:0]: VS width
08	RSVD	XX	–	Reserved
09	COM2	00	RW	Common Control 2 Bit[7:5]: Always precharge Bit[4]: Sleep mode enable (SCCB standby enable) 0: Normal mode 1: Sleep mode Bit[3]: Pin D0 output control 0: D0 1: STROBE Bit[2]: Reserved Bit[1:0]: Output drive current select 00: Weakest 01: Double capability 10: Double capability 11: Triple drive current
0A	PID	96	R	Product ID Number MSB (Read only)
0B	VER	63	R	Product ID Number LSB (Read only)
0C	COM3	38	RW	Common Control 3 Bit[7:3]: Reserved Bit[2]: Manually set banding 0: 60 Hz 1: 50 Hz Bit[1]: Auto set banding Bit[0]: Snapshot option 0: Enable live video output after snapshot sequence 1: Output single frame only
0D-0E	RSVD	XX	–	Reserved

Table 5 Device Control Register List (Sheet 3 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0F	COM6	46	RW	Common Control 6 Bit[7:4]: Reserved Bit[3]: Night mode enable 0: Disable 1: Enable Bit[2:0]: Reserved
10	AEC	00	RW	Automatic Exposure Control - AEC[9:2] (see register REG45[5:0] for AEC[15:10] and register REG04 for AEC[1:0]) AEC[15:0]: Exposure time TEX = tLINE x AEC[15:0] ***NOTE**: The maximum exposure time is 1 frame period even if TEX is longer than 1 frame period*
11	CLKRC	80	RW	Clock Rate Control Bit[7:6]: Reserved Bit[5:0]: Clock divider for frame rate adjustment CLK = XVCLK / (decimal value of CLKRC[5:0] + 1)
12	COM7	00	RW	Common Control 7 Bit[7]: SRST 1: Initiates soft reset. All registers are set to factory default values after which the chip resumes normal operation Bit[6:5]: Resolution selection 00: SXGA (full size) mode 01: Not used 10: VGA mode 11: Not used Bit[4:3]: Reserved Bit[2]: Zoom mode Bit[1:0]: Reserved
13	COM8	E7	RW	Common Control 8 Bit[7]: Reserved Bit[6]: AEC step size limit Bit[5]: Banding filter selection 0: OFF 1: ON, set minimum exposure to 1/120s or 1/100s Bit[4:3]: Reserved Bit[2]: AGC auto/manual control selection 0: Manual 1: Auto Bit[1]: AWB auto/manual control selection 0: Manual 1: Auto Bit[0]: Exposure control 0: Manual 1: Auto

Table 5 Device Control Register List (Sheet 4 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
14	COM9	40	RW	Common Control 9 Bit[7:5]: AGC gain ceiling 000: 2x 001: 4x 010: 8x 011: 16x 100: 32x 101: Not used 110: Not used 111: Not used Bit[4]: Reserved Bit[3]: Exposure time can be less than limitation of banding filter (1/120s or 1/100s) when light is too strong Bit[2]: Data output format - VSYNC drop option 0: VSYNC always exists 1: VSYNC will drop when frame data drops Bit[1]: Enable drop frame when AEC step is larger than the exposure gap Bit[0]: Reserved
15	COM10	00	RW	Common Control 10 Bit[7:6]: Reserved Bit[5]: PCLK output selection (works on row data output) 0: PCLK always output 1: PCLK output qualified by HREF Bit[4:2]: Reserved Bit[1]: VSYNC polarity 0: Positive 1: Negative Bit[0]: Reserved
16	GREEN	40	RW	Green Gain Control
17	HREFST	0D	RW	Horizontal Window Start 8 MSBs (3 LSBs in register REG32[2:0]) Bit[10:0]: Select beginning of horizontal window, each LSB represents two pixels
18	HREFEND	5D	RW	Horizontal Window End 8 MSBs (3 LSBs in register REG32[5:3]) Bit[10:0]: Select end of horizontal window, each LSB represents two pixels
19	VSTRT	01	RW	Vertical Window Line Start 8 MSBs (2 LSBs are in register COM1[1:0]) Bit[9:0]: Select start of vertical window, each LSB represents two scan lines
1A	VEND	82	RW	Vertical Window Line End 8 MSBs (2 LSBs are in register COM1[3:2]) Bit[9:0]: Select end of vertical window, each LSB represents two scan lines
1B	RSVD	XX	–	Reserved
1C	MIDH	7F	R	Manufacturer ID Byte – High (Read only = 0x7F)
1D	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)

Table 5 Device Control Register List (Sheet 5 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
1E	REG1E	F9	RW	Register 1E Bit[7]: White defect pixel correction 0: Disable 1: Enable Bit[6]: Black defect pixel correction 0: Disable 1: Enable Bit[5:0]: Reserved
1F-23	RSVD	XX	–	Reserved
24	AEW	78	RW	Luminance Signal High Range for AEC/AGC Operation AEC/AGC value decreases in auto mode when average luminance is greater than AEW[7:0]
25	AEB	68	RW	Luminance Signal Low Range for AEC/AGC Operation AEC/AGC value increases in auto mode when average luminance is less than AEB[7:0]
26	VV	D4	RW	Fast Mode Large Step Range Thresholds (effective only in AEC/AGC fast mode) Bit[7:4]: High threshold Bit[3:0]: Low threshold AEC/AGC may change in larger steps when luminance average is greater than VV[7:4] or less than VV[3:0]
27-29	RSVD	XX	–	Reserved
2A	REG2A	00	RW	Common Control 2A Bit[7:4]: Line interval adjustment value 4 MSBs (see register REG2B[7:0] for 8 MSBs) Bit[3:2]: HSYNC timing end point adjustment 2 MSBs (see register HEDY for 8 LSBs) Bit[1:0]: HSYNC timing start point adjustment 2 MSBs (see register HSDY for 8 LSBs)
2B	REG2B	00	RW	Common Control 2B Bit[7:0]: Line interval adjustment value 8 LSBs (see register REG2A[7:4] for 4 MSBs) The frame rate will be adjusted by changing the line interval. Each LSB will add 1/1520 Tframe in SXGA and 1/760 Tframe in VGA mode to the frame period.
2C	RSVD	XX	–	Reserved
2D	ADDVSL	00	RW	VSYNC Pulse Width 8 LSBs Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is 4 x tline. Each LSB count will add 1 x tline to the VSYNC active period.
2E	ADDVSH	00	RW	VSYNC Pulse Width 8 MSBs Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is 4 x tline. Each MSB count will add 256 x tline to the VSYNC active period.

Table 5 Device Control Register List (Sheet 6 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
2F	YAVG	00	R	Luminance Average (this register will auto update)
30	HSDY	08	RW	HSYNC Position and Width Start 8 LSBs This register and register REG2A[1:0] define the HSYNC start position. Each LSB will shift the HSYNC starting point by a 2 pixel period.
31	HEDY	20	RW	HSYNC Position and Width End 8 LSBs This register and register REG2A[3:2] define the HSYNC end position. Each LSB will shift the HSYNC starting point by a 2 pixel period.
32	REG32	24	RW	Common Control 32 Bit[7:6]: Pixel clock divide option 00: No effect on PCLK 01: No effect on PCLK 10: PCLK frequency divide by 2 11: PCLK frequency divide by 4 Bit[5:3]: Horizontal window end position 3 LSBs (8 LSBs in register HREFEND) Bit[2:0]: Horizontal window start position 3 LSBs (8 LSBs in register HREFST)
33	REG33	C0	RW	Register 33 Bit[7:4]: Reserved Bit[3]: Mirror function (used with register bit REG04[7] (0x04)) Bit[2:0]: Reserved
34-35	RSVD	XX	–	Reserved
36	REG36	94	RW	Register 36 Bit[7:6]: Reserved Bit[5]: Auto de-noise divider value 0: 128 1: 64 Bit[4:0]: Reserved
37-3A	RSVD	XX	–	Reserved
3B	REG3B	00	RW	Power Control 3B Bit[7:4]: Reserved Bit[3]: Bypass internal regulator 0: Use internal regulator to generate V_{DD-D} power 1: Bypass internal regulator (V_{DD-D} power needs to be provided by an external source) Bit[2:0]: Reserved
3C	RSVD	XX	–	Reserved
3D	REG3D	3C	RW	Common Control 3D Bit[7:6]: Reserved Bit[5:0]: PLL divider f_{CLK} = XCLK × (0x40 – REG3D[5:0]) / 8 / (CLKRC[5:0] + 1)

Table 5 Device Control Register List (Sheet 7 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
3E	REG3E	50	RW	Register 3E Bit[7]: PLL bypass option 0: Enable PLL 1: Bypass PLL Bit[6:0]: Reserved
3F-40	RSVD	XX	–	Reserved
41	REG41	00	RW	Register 41 Bit[7:5]: UV adjust offset value[5:3] between gain threshold 1 and gain threshold 2. For others, refer to register REG5B[4:2] (0x5B). Bit[4:0]: Reserved
42	RSVD	XX	–	Reserved
43	REG43	00	RW	Register 43 Bit[7]: 9-zone average AEC option 0: Full size and VGA30 1: Other size Bit[6:0]: Reserved
44	RSVD	XX	–	Reserved
45	REG45	00	RW	Register 45 Bit[7:6]: AGC[9:8], AGC highest gain control Bit[5:0]: AEC[15:10], AEC 6 MSBs (see register AEC for AEC[9:2] and register REG04 for AEC[1:0]).
46	FLL	00	RW	Frame Length Adjustment 8 LSBs Each bit will add 1 horizontal line timing in frame
47	FLH	00	RW	Frame Length Adjustment 8 MSBs Each bit will add 256 horizontal lines timing in frame
48-4A	RSVD	XX	–	Reserved
4B	COM22	00	RW	Common Control 22 Bit[7:0]: Flash light control
4C-4D	RSVD	XX	–	Reserved
4E	COM25	05	RW	Common Control 25 Bit[7:6]: 50 Hz banding AEC 2 MSBs Bit[5:4]: 60 Hz banding AEC 2 MSBs Bit[3:0]: Reserved
4F	BD50	9E	RW	50 Hz Banding AEC 8 LSBs (see register COM25[7:6] for 2 MSBs)
50	BD60	84	RW	60 Hz Banding AEC 8 LSBs (see register COM25[5:4] for 2 MSBs)
51-59	RSVD	XX	–	Reserved
5A	REG5A	57	RW	Register 5A Bit[7:4]: 50 Hz banding maximum AEC step Bit[3:0]: 60 Hz banding maximum AEC step

Table 5 Device Control Register List (Sheet 8 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
5B	REG5B	20	RW	Register 5B Bit[7:5]: Reserved Bit[4:2]: UV adjust offset value[5:3] between gain threshold 1 and gain threshold 2. For others, refer to register REG41[7:5] (0x41). Bit[1:0]: Reserved
5C	REG5C	00	RW	Register 5C Bit[7]: Average AEC option 0: 9-zone average AEC 1: Full average AEC Bit[6:0]: Reserved
5D	REG5D	55	RW	9-zone Average Weight Option - AVGsel[7:0]
5E	REG5E	55	RW	9-zone Average Weight Option - AVGsel[15:8]
5F	REG5F	21	RW	Register 5F Bit[7:2]: Reserved Bit[1:0]: 9-zone average weight option - AVGsel[17:16]
60	REG60	80	RW	Register 60 Bit[7:3]: Reserved Bit[2:0]: UV adjust slope[2:0] between gain threshold 1 and gain threshold 2. For others, refer to registers COM1[5:4] (0x03) and REG05[2:0] (0x05).
61	HISTO_LOW	80	RW	Histogram Algorithm Low Level Bit[7:0]: Histogram algorithm low level
62	HISTO_HIGH	90	RW	Histogram Algorithm High Level Bit[7:0]: Histogram algorithm high level
63	REG63	01	RW	Register 63 Bit[7:6]: Reserved Bit[5]: Raw data output format (valid when register REG07[1:0] is 2'b11) 0: DSP function (AWB and Gamma) works on Raw output data 1: DSP functions do not work on Raw output data Bit[4:0]: Reserved
64	REG64	20	RW	Register 64 Bit[7]: BLC line select 0: SXGA 1: Other resolution Bit[6:0]: Reserved
65	REG65	10	RW	Register 65 Bit[7:2]: Reserved Bit[1:0]: UV adjustment gain threshold 2 value[4:3]

Table 5 Device Control Register List (Sheet 9 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
66	REG66	00	RW	Register 66 Bit[7:5]: UV adjustment gain threshold 2 value[2:0] Bit[4:0]: Reserved
67-69	RSVD	XX	–	Reserved
6A	REG6A	24	RW	Register 6A Bit[7:5]: Reserved Bit[4]: FIFO manual option (works with scaling function) 0: Auto mode 1: Manual mode Bit[3:0]: Reserved
6B-74	RSVD	XX	–	Reserved
75	REG75	D0	RW	Histogram-based AEC Lower Limit of Probability - LPH
76	REG76	D0	RW	Histogram-based AEC Upper Limit of Probability - UPL
77	REG77	F0	RW	Histogram-based AEC Probability Threshold for LRL - TPL
78	REG78	90	RW	Histogram-based AEC Probability Threshold for HRL - TPH
79	REG79	E5	RW	Register 79 Bit[7:2]: High nibble of luminance thrreshold for AEC/AGC speed control Bit[3:0]: Low nibble of luminance threshold for AEC/AGC speed control
7A-7B	RSVD	XX	–	Reserved
7C	REG7C	05	RW	Register 7C Bit[7]: AEC option 0: Average-based AEC 1: Histogram-based AEC Bit[6:0]: Reserved
7D	REG7D	00	RW	Lens Correction Center Coordinates X Bit[7]: Sign bit Bit[6:0]: X-coordinate for lens correction center
7E	REG7E	00	RW	Lens Correction Center Coordinates Y Bit[7]: Sign bit Bit[6:0]: Y-coordinate for lens correction center
7F	REG7F	18	RW	Radius of the Circular Section Where Lens Correction Is Not Needed
80	REG80	04	RW	Lens Correction Blue Gain Parameter - this register is valid when register LC7[2] (0x83) = 1
81	REG81	04	RW	Lens Correction Red Gain Parameter - this register is valid when register LC7[2] (0x83) = 1
82	REG82	04	RW	Lens correction Green Gain Parameter

Table 5 Device Control Register List (Sheet 10 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
83	LC7	06	RW	Bit[7:3]: Reserved Bit[2]: Lens correction control select 0: Use register REG82 (0x82) for gain parameter for R, G, and B channels 1: Use register REG82 (0x82) for green gain parameter, register REG80 (0x80) for blue gain parameter, and register REG81 (0x81) for red gain parameter Bit[1]: Reserved Bit[0]: Lens correction enable switch 0: Disable 1: Enable
84	REG84	86	RW	De-noise Level
85	REG85	E7	RW	Register 85 Bit[7:5]: Reserved Bit[4]: RAW/YUV (only works when register bits REGD7[1:0] (0xD7) = 0'b10) Bit[3]: FIFO enable (works with scaling function) Bit[2]: Gamma enable option 0: Disable 1: Enable Bit[1]: AWB gain Bit[0]: AWB
86-87	RSVD	XX	–	Reserved
88	REG08	A2	RW	Register 88 Bit[7:5]: AWB option 0: Advanced AWB 1: Simple AWB Bit[6:0]: Reserved
89-9A	RSVD	XX	–	Reserved
9B	GAM1	04	RW	Gamma Curve Segment 1 End Point
9C	GAM2	07	RW	Gamma Curve Segment 2 End Point
9D	GAM3	10	RW	Gamma Curve Segment 3 End Point
9E	GAM4	28	RW	Gamma Curve Segment 4 End Point
9F	GAM5	36	RW	Gamma Curve Segment 5 End Point
A0	GAM6	44	RW	Gamma Curve Segment 6 End Point
A1	GAM7	52	RW	Gamma Curve Segment 7 End Point
A2	GAM8	60	RW	Gamma Curve Segment 8 End Point
A3	GAM9	6C	RW	Gamma Curve Segment 9 End Point
A4	GAM10	78	RW	Gamma Curve Segment 10 End Point
A5	GAM11	8C	RW	Gamma Curve Segment 11 End Point

Table 5 Device Control Register List (Sheet 11 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
A6	GAM12	9E	RW	Gamma Curve Segment 12 End Point
A7	GAM13	BB	RW	Gamma Curve Segment 13 End Point
A8	GAM14	D2	RW	Gamma Curve Segment 14 End Point
A9	GAM15	E5	RW	Gamma Curve Segment 15 End Point
AA	SLOP	24	RW	Gamma Curve Segment 15 Slope
AB	REGAB	E7	RW	Register AB Bit[7:4]: Reserved Bit[3]: Scaling enable option 0: Disable 1: Enable Bit[2]: Sharpness enable option 0: Disable 1: Enable Bit[1]: De-noise enable option 0: Disable 1: Enable Bit[0]: Reserved
AC	REGAC	02	RW	De-noise Offset Limit in Auto De-noise Mode
AD	REGAD	25	RW	Register AD Bit[7:5]: Reserved Bit[4:0]: Sharpness value when GAIN < 2x
AE	REGAE	20	RW	Register AE Bit[7:3]: Reserved Bit[2]: Sharpness threshold double Bit[1:0]: Reserved
AF	RSVD	XX	–	Reserved
B0	REGB0	43	RW	Register B0 Bit[7]: Manual de-noise mode enable 0: Auto de-noise mode 1: Manual de-noise Bit[6:0]: Reserved
B1-B6	RSVD	XX	–	Reserved
B7	REGB7	00	RW	Register B7 Bit[7]: Scaling mode vertical output size bit[0] (11 bits total). For others, refer to registers REGB8[7:6] and REGBC Bit[6:4]: Scaling mode horizontal output size bit[2:1] (11 bits total). For others, refer to register REGBB Bit[3:0]: Reserved

Table 5 Device Control Register List (Sheet 12 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
B8	REGB8	00	RW	Register B8 Bit[7:6]: Scaling mode vertical output size bit[2:1] (11 bits total). For others, refer to registers REGB7[7] and REGBC Bit[5:3]: Scaling mode vertical input size bit[2:0] (11 bits total). For others, refer to register REGBA Bit[2:0]: Scaling mode horizontal input size bit[2:0] (11 bits total). For others, refer to register REGB9
B9	REGB9	A0	RW	Scaling Mode Horizontal Input Size bit[10:3] (11 bits total). For others, refer to register REGB8[2:0]
BA	REGBA	80	RW	Scaling Mode Vertical Input Size bit[10:3] (11 bits total). For others, refer to register REGB8[5:3]
BB	REGBB	A0	RW	Scaling Mode Horizontal Output Size[10:3] (11 bits total). For others, refer to registers REGB8[7:6] and REGB7[6:4]
BC	REGBC	80	RW	Scaling Mode Vertical Output Size[10:3] (11 bits total). For others refer to registers REGB7[7] and REGB8[7:6]
BD	CMX1	05	RW	Color Matrix Parameter 1
BE	CMX2	16	RW	Color Matrix Parameter 2
BF	CMX3	05	RW	Color Matrix Parameter 3
BD–BF				Y = (CMX1 × R + CMX2 × G + CMX3 × B) / 32
C0	CMX4	07	RW	Color Matrix Parameter 4
C1	CMX5	18	RW	Color Matrix Parameter 5
C2	CMX6	1F	RW	Color Matrix Parameter 6
C0–C2				U = (CMX4 × R + CMX5 × G + CMX6 × B) / 32
C3	CMX7	2B	RW	Color Matrix Parameter 7
C4	CMX8	2B	RW	Color Matrix Parameter 8
C5	CMX9	00	RW	Color Matrix Parameter 9
C3–C5				V = (CMX7 × R + CMX8 × G + CMX9 × B) / 32
C6	CMX10	98	RW	Color Matrix Control 1 Bit[7]: Sign bit of CMX8 Bit[6]: Sign bit of CMX7 Bit[5]: Sign bit of CMX6 Bit[4]: Sign bit of CMX5 Bit[3]: Sign bit of CMX4 Bit[2]: Sign bit of CMX3 Bit[1]: Sign bit of CMX2 Bit[0]: Sign bit of CMX1

Table 5 Device Control Register List (Sheet 13 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
C7	CMX11	10	RW	Color Matrix Control 2 Bit[7]: Sign bit of CMX9 Bit[6]: Reserved Bit[5]: Auto UV adjustment enable 0: Disable 1: Enable Bit[4]: Special Digital Effects (SDE) enable 0: Disable 1: Enable Bit[3:0]: Reserved
C8	REGC8	02	RW	Register C8 Bit[7]: Fixed Y output value 0: Disable 1: Enable Bit[6]: Negative output 0: Disable 1: Enable Bit[5]: Gray scale output 0: Disable 1: Enable Bit[4]: Fixed V output value 0: Disable 1: Enable Bit[3]: Fixed U output value 0: Disable 1: Enable Bit[2]: Contrast function enable 0: Disable 1: Enable Bit[1]: Color saturation function enable 0: Disable 1: Enable Bit[0]: Hue adjustment enable 0: Disable 1: Enable
C9	REGC9	80	RW	Hue Adjustment Cosine Parameter
CA	REGCA	00	RW	Hue Adjustment Sine Parameter
CB	REGCB	40	RW	Saturation U Gain Value
CC	REGCC	40	RW	Saturation V Gain Value
CD	REGCD	80	RW	Fixed U Output Value
CE	REGCE	80	RW	Fixed V Output Value

Table 5 Device Control Register List (Sheet 14 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
CF	REGCF	00	RW	Y Offset Value
D0	REGD0	20	RW	Y Gain Value
D1	REGD1	00	RW	Y Brightness Value
				Y' = [(Y + Yoffset) × Ygain] + Ybrightness when enabling contrast function
D2	REGD2	00	RW	Register D2 Bit[7]: Auto UV adjustment enable Bit[6:5]: Reserved Bit[4:0]: UV adjust offset value after gain threshold 2
D3	REGD3	00	RW	FIFO Delay Timing Configuration (works with scaling function)
D4	RSVD	XX	–	Reserved
D5	REGD5	00	RW	IO Pad Direction Control Bit[7]: D7 direction control 0: Input 1: Output Bit[6]: D6 direction control 0: Input 1: Output Bit[5]: D5 direction control 0: Input 1: Output Bit[4]: D4 direction control 0: Input 1: Output Bit[3]: D3 direction control 0: Input 1: Output Bit[2]: D2 direction control 0: Input 1: Output Bit[1]: D1 direction control 0: Input 1: Output Bit[0]: D0 direction control 0: Input 1: Output
D6	REGD6	00	RW	Register D6 Bit[7:2]: Reserved Bit[1]: D9 direction control 0: Input 1: Output Bit[0]: D8 direction control 0: Input 1: Output

Table 5 Device Control Register List (Sheet 15 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
D7	REGD7	10	RW	Register D7 Bit[7:5]: Reserved Bit[4]: YU swap function 0: U Y V Y 1: Y U Y V Bit[3]: Data pins swap function (changes MSB to D0 and LSB to D9) - works in YUV mode 0: Disable 1: Enable Bit[2]: HREF to HSYNC 0: Output HREF signal 1: Output HSYNC signal Bit[1:0]: Data output format selection 00: YUV output 01: RGB output 10: ISP RAW output 11: RAW output
D8	REGD8	C4	RW	Register D8 Bit[7:6]: Reserved Bit[5]: HREF/HSYNC negative output 0: Positive output 1: Negative output Bit[4]: Reserved Bit[3]: CCIR656 output selection 0: Disable 1: Enable Bit[2]: Reserved Bit[1:0]: RGB data output format selection (effective when register bits REGD7[1:0] = 01) 00: Not used 01: RGB565 10: RGB555 11: RGB444
D9	REGD9	64	RW	Register D9 Bit[7:4]: Sharpness value when 4x < GAIN < 8x Bit[3:0]: Sharpness value when 2x < GAIN < 4x
DA	REGDA	86	RW	Register DA Bit[7:4]: Sharpness value when 16x < GAIN Bit[3:0]: Sharpness value when 8x < GAIN < 16x
DB-DE	RSVD	XX	–	Reserved
NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.				

Package Specifications

The OV9660 uses a 26-pin Chip Scale Package 2 (CSP2). Refer to Figure 11 for package information, Table 6 for package dimensions and Figure 12 for the array center on the chip.

Note: For OVT devices that are lead-free, all part marking letters are lower case. Underlining the last digit of the lot number indicates CSP2 is used.

Figure 11 OV9660 Package Specifications

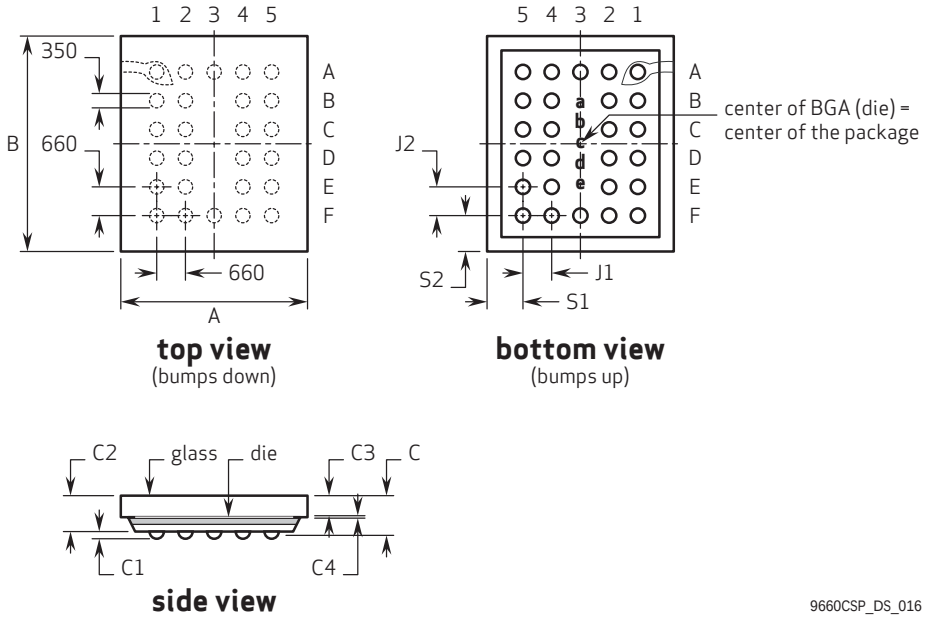
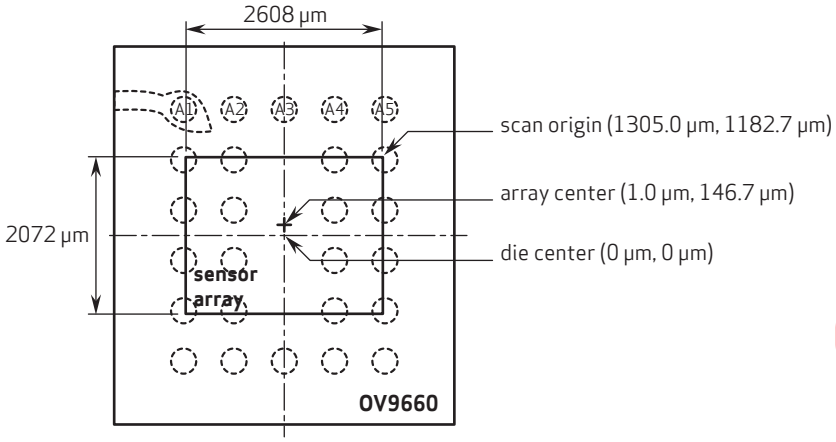


Table 6 CSP Package Dimensions

Parameter	Symbol	Min	Nominal	Max	Unit
Package body dimension X	A	4460	4485	4510	µm
Package body dimension Y	B	4960	4985	5010	µm
Package height	C	845	905	965	µm
Ball height	C1	150	180	210	µm
Package body thickness	C2	680	725	770	µm
Cover glass thickness	C3	375	400	425	µm
Airgap between cover glass and sensor	C4	30	45	60	µm
Ball diameter	D	320	350	380	µm
Total pin count	N		26		
Pin count X-axis	N1		5		
Pin count Y-axis	N2		6		
Pins pitch X-axis	J1		660		µm
Pins pitch Y-axis	J2		660		µm
Edge-to-pin center distance analog X	S1	893	923	953	µm
Edge-to-pin center distance analog Y	S2	813	843	873	µm

Sensor Array Center

Figure 12 OV9660 Sensor Array Center



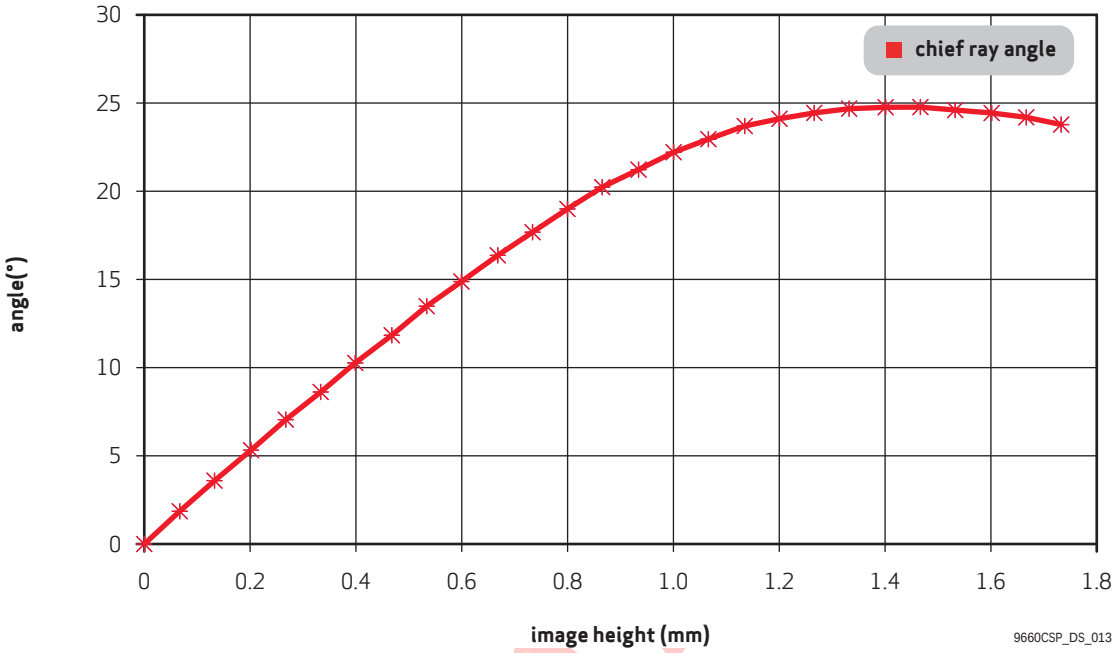
note1 this drawing is not to scale and is for reference only.

note2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pin A1 oriented down on the PCB.

9660COB_DS_017

Chief Ray Angle

Figure 13 OV9660 Chief Ray Angle



IR Reflow Ramp Rate Requirements

OV9660 Lead-Free Packaged Devices

Note: For OVT devices that are lead-free, all part marking letters are lower case.

Figure 14 IR Reflow Ramp Rate Requirements

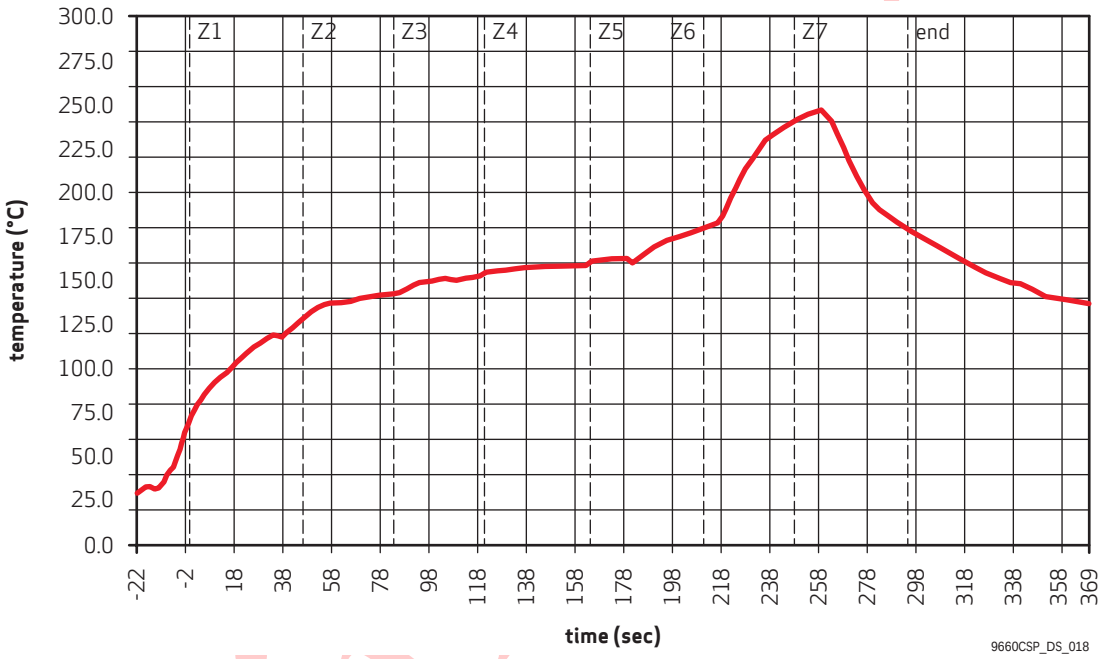


Table 7 Reflow Conditions

Condition	Exposure
Average ramp-up rate (30°C to 217°C)	Less than 3°C per second
> 100°C	Between 330 - 600 seconds
> 150°C	At least 210 seconds
> 217°C	At least 30 seconds (30 ~ 120 seconds)
Peak temperature	245°C
Cool-down rate (peak to 50°C)	Less than 6°C per second
Time from 30°C to 245°C	No greater than 390 seconds

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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REVISION CHANGE LIST

Document Title: OV9660 (CSP2) Datasheet **Version:** 1.0

DESCRIPTION OF CHANGES

- Initial Release

REVISION CHANGE LIST

Document Title: OV9660 (CSP2) Datasheet **Version:** 1.1

DESCRIPTION OF CHANGES

- Under Key Specifications on page 1, changed specification for Image Area from "2608 µm x 2080 µm" to "2608 µm x 2072 µm"
- In Figure 17 on page 21, changed sensor array center coordinates from "(1.0 µm, 150.7 µm)" to "(1.0 µm, 146.7 µm)"
- In Figure 17 on page 21, changed scan origin coordinates from "(1305.0 µm, 1190.7 µm)" to "(1305.0 µm, 1182.7 µm)"
- In Figure 17 on page 21, changed height of the image array from "2080 µm" to "2072 µm"

REVISION CHANGE LIST

Document Title: OV9660 (CSP2) Datasheet **Version:** 1.2

DESCRIPTION OF CHANGES

- On page 1, changed the document title from “OV9660 Color CMOS SXGA (1.3 MegaPixel CAMERACHIP™ Sensor with OmniPixel3™ Technology” to “OV9660 Color CMOS SXGA (1.3 MegaPixel CAMERACHIP™ Sensor with OmniPixel2™ Technology”
- Changed all instances of OmniPixel3 to OmniPixel2 in the headers of the even pages and in the footer of the first page

REVISION CHANGE LIST

Document Title: OV9660 (CSP2) Datasheet **Version:** 1.3

DESCRIPTION OF CHANGES

The following changes were made to version 1.2:

- In Table 5 on page 14, changed name, default value, R/W and description of register 0x01 from “RSVD”, “XX”, “–” and “Reserved” to “BLUE”, “40”, “RW” and “Blue Gain Control”, respectively
- In Table 5 on page 14, changed name, default value, R/W and description of register 0x02 from “RSVD”, “XX”, “–” and “Reserved” to “RED”, “40”, “RW” and “Red Gain Control”, respectively
- In Table 5 on page 14, added “ - effective when register bit COM6[3] = 1 (0x0F) (night mode enable)” to description of register bits COM1[7:6] (0x03)
- In Table 5 on page 16, changed description of register bits COM7[6:5] (0x12) from:

  Bit[6:5]: Resolution selection
  00: SXGA (full size) mode
  01: VGA mode
  10: QVGA mode
  11: Not used

  to:

  Bit[6:5]: Resolution selection
  00: SXGA (full size) mode
  01: VGA mode
  10: Not used
  11: Not used
- In Table 5 on page 16, changed description of register bit COM8[1] (0x13) from “Reserved” to:

  Bit[1]: AWB auto/manual control selection
  0: Manual
  1: Auto
- In Table 5 on page 17, changed description of register bits COM10[7:6] (0x15) from:

  Bit[7]: CHSYNC pin output swap
  0: CHSYNC
  1: HREF
  Bit[6]: HREF pin output swap
  0: HREF
  1: CHSYNC

  to:

  Bit[7:6]: Reserved
- In Table 5 on page 17, changed name, default value, R/W and description of register 0x16 from “RSVD”, “XX”, “–” and “Reserved” to “GREEN”, “40”, “RW” and “Green Gain Control”, respectively

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 5 on page 17, changed default value of register HREFST (0x17) from “0B” to “0D”
- In Table 5 on page 17, changed default value of register HREFEND (0x18) from “5B” to “5D”
- In Table 5 on page 17, changed default value of register VEND (0x1A) from “81” to “82”
- In Table 5 on page 18, changed name, default value, and R/W of register 0x1E from “RSVD”, “XX” and “–” to “REG1E”, “C8”, and “RW”, respectively
- In Table 5 on page 18, changed decription of register 0x1E from “Reserved” to:

  Register 1E
  - Bit[7]: White defect pixel correction
    - 0: Disable
    - 1: Enable
  - Bit[6]: Black defect pixel correction
    - 0: Disable
    - 1: Enable
  - Bit[5:0]: Reserved
- In Table 5 on page 19, changed default value of register REG32 (0x32) from “00” to “24”
- In Table 5 on page 19, changed name, default value, and R/W of register 0x33 from “RSVD”, “XX” and “–” to “REG33”, “00”, and “RW”, respectively
- In Table 5 on page 19, changed decription of register 0x33 from “Reserved” to:

  Register 33
  - Bit[7:4]: Reserved
  - Bit[3]: Mirror function (used with register bit REG04[7] (0x04))
  - Bit[2:0]: Reserved
- In Table 5 on page 19, changed name, default value, and R/W of register 0x3B from “RSVD”, “XX” and “–” to “REG3B”, “40”, and “RW”, respectively
- In Table 5 on page 19, changed decription of register 0x3B from “Reserved” to:

  Power Control 3B
  - Bit[7:4]: Reserved
  - Bit[3]: Bypass internal regulator
    - 0: Use internal regulator to generate V_{DD-D} power
    - 1: Bypass internal regulator (V_{DD-D} power needs to be provided by an external source)
  - Bit[2:0]: Reserved
- In Table 5 on page 20, changed name, default value, R/W and description of register 0x48 to “RSVD”, “XX”, “–” and “Reserved”, respectively
- In Table 5 on page 20, changed name, default value, R/W and description of register 0x49 to “RSVD”, “XX”, “–” and “Reserved”, respectively
- In Table 5 on page 20, changed name, default value, and R/W of register 0x5F from “RSVD”, “XX” and “–” to “REG5F”, “21”, and “RW”, respectively

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 5 on page 20, changed decription of register 0x5F from “Reserved” to:

  Register 5F
  - Bit[7:2]: Reserved
  - Bit[1:0]: 9-zone average weight option - AVGsel[17:16]

- In Table 5 on page 20, changed name, default value, and R/W of register 0x63 from “RSVD”, “XX” and “–” to “REG63”, “01”, and “RW”, respectively
- In Table 5 on page 20, changed decription of register 0x63 from “Reserved” to:

  Register 63
  - Bit[7:6]: Reserved
  - Bit[5]: Raw data output format (valid when register REG07[1:0] is 2’b11)
    - 0: DSP function (AWB and Gamma) works on Raw output data
    - 1: DSP functions do not work on Raw output data
  - Bit[4:0]: Reserved

- In Table 5 on page 20, changed name, default value, and R/W of register 0x7C from “RSVD”, “XX” and “–” to “REG7C”, “05”, and “RW”, respectively
- In Table 5 on page 20, changed decription of register 0x7C from “Reserved” to:

  Register 7C
  - Bit[7]: AEC option
    - 0: Average-based AEC
    - 1: Histogram-based AEC
  - Bit[6:0]: Reserved

- In Table 5 on page 20, changed name, default value, and R/W of register 0x83 from “RSVD”, “XX” and “–” to “LC7”, “06”, and “RW”, respectively
- In Table 5 on page 20, changed decription of register 0x83 from “Reserved” to:

  Bit[7:1]: Reserved

  Bit[0]: Lens correction enable switch
  - 0: Disable
  - 1: Enable

- In Table 5 on page 21, changed name and default value of register 0x85 from “ISPCOM1” and “03” to “REG85” and “E7”, respectively
- In Table 5 on page 21, changed description of register bit REG85[2] (0x85) from “Reserved” to:

  Bit[2]: Gamma enable option
  - 0: Disable
  - 1: Enable

- In Table 5 on page 21, changed name, default value, and R/W of register 0x88 from “RSVD”, “XX” and “–” to “REG88”, “A2”, and “RW”, respectively
- In Table 5 on page 21, changed decription of register 0x88 from “Reserved” to:

  Register 88
  - Bit[7:5]: AWB option
    - 0: Advanced AWB
    - 1: Simple AWB
  - Bit[6:0]: Reserved

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 5 on page 21, changed name, default value, R/W and description of register 0x9B from “RSVD”, “XX”, “–” and “Reserved” to “GAM1”, “0E”, “RW” and “Gamma Curve Segment 1 End Point”, respectively
- In Table 5 on page 21, changed name, default value, R/W and description of register 0x9C from “RSVD”, “XX”, “–” and “Reserved” to “GAM2”, “1A”, “RW” and “Gamma Curve Segment 2 End Point”, respectively
- In Table 5 on page 21, changed name, default value, R/W and description of register 0x9D from “RSVD”, “XX”, “–” and “Reserved” to “GAM3”, “31”, “RW” and “Gamma Curve Segment 3 End Point”, respectively
- In Table 5 on page 21, changed name, default value, R/W and description of register 0x9E from “RSVD”, “XX”, “–” and “Reserved” to “GAM4”, “5A”, “RW” and “Gamma Curve Segment 4 End Point”, respectively
- In Table 5 on page 21, changed name, default value, R/W and description of register 0x9F from “RSVD”, “XX”, “–” and “Reserved” to “GAM5”, “69”, “RW” and “Gamma Curve Segment 5 End Point”, respectively
- In Table 5 on page 21, changed name, default value, R/W and description of register 0xA0 from “RSVD”, “XX”, “–” and “Reserved” to “GAM6”, “75”, “RW” and “Gamma Curve Segment 6 End Point”, respectively
- In Table 5 on page 21, changed name, default value, R/W and description of register 0xA1 from “RSVD”, “XX”, “–” and “Reserved” to “GAM7”, “7E”, “RW” and “Gamma Curve Segment 7 End Point”, respectively
- In Table 5 on page 21, changed name, default value, R/W and description of register 0xA2 from “RSVD”, “XX”, “–” and “Reserved” to “GAM8”, “88”, “RW” and “Gamma Curve Segment 8 End Point”, respectively
- In Table 5 on page 21, changed name, default value, R/W and description of register 0xA3 from “RSVD”, “XX”, “–” and “Reserved” to “GAM9”, “8F”, “RW” and “Gamma Curve Segment 9 End Point”, respectively
- In Table 5 on page 21, changed name, default value, R/W and description of register 0xA4 from “RSVD”, “XX”, “–” and “Reserved” to “GAM10”, “96”, “RW” and “Gamma Curve Segment 10 End Point”, respectively
- In Table 5 on page 21, changed name, default value, R/W and description of register 0xA5 from “RSVD”, “XX”, “–” and “Reserved” to “GAM11”, “A3”, “RW” and “Gamma Curve Segment 11 End Point”, respectively
- In Table 5 on page 21, changed name, default value, R/W and description of register 0xA6 from “RSVD”, “XX”, “–” and “Reserved” to “GAM12”, “AF”, “RW” and “Gamma Curve Segment 12 End Point”, respectively
- In Table 5 on page 21, changed name, default value, R/W and description of register 0xA7 from “RSVD”, “XX”, “–” and “Reserved” to “GAM13”, “C4”, “RW” and “Gamma Curve Segment 13 End Point”, respectively

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 5 on page 21, changed name, default value, R/W and description of register 0xA8 from “RSVD”, “XX”, “–” and “Reserved” to “GAM14”, “D7”, “RW” and “Gamma Curve Segment 14 End Point”, respectively
- In Table 5 on page 21, changed name, default value, R/W and description of register 0xA9 from “RSVD”, “XX”, “–” and “Reserved” to “GAM15”, “E8”, “RW” and “Gamma Curve Segment 15 End Point”, respectively
- In Table 5 on page 21, changed name, default value, R/W and description of register 0xAA from “RSVD”, “XX”, “–” and “Reserved” to “SLOP”, “20”, “RW” and “Gamma Curve Segment 15 Slope”, respectively
- In Table 5 on page 22, changed name and default value of register 0xAB from “ISPCOM2” and “07” to “REGAB” and “E7”, respectively
- In Table 5 on page 22, changed description of register 0xAB from:

  Bit[7:5]: Reserved
  Bit[4]: Scaling man enable option
  0: Disable
  1: Enable
  Bit[3]: Scaling enable option
  0: Disable
  1: Enable
  Bit[2:0]: Reserved

  to:

  Register AB
  Bit[7:4]: Reserved
  Bit[3]: Scaling man enable option
  0: Disable
  1: Enable
  Bit[2]: Scaling enable option
  0: Disable
  1: Enable
  Bit[1]: De-noise enable option
  0: Disable
  1: Enable
  Bit[0]: Reserved
- In Table 5 on page 22, changed name, default value, R/W and description of register 0xB5 to “RSVD”, “XX”, “–” and “Reserved”, respectively
- In Table 5 on page 22, changed name of register 0xB7 from “SCALEHVH” to “REGB7”
- In Table 5 on page 22, changed description of register bits REGB7[7:4] (0xB7) from:

  Bit[7:4]: Reserved
  Bit[3:2]: Scaling man mode vertical scale factor high 2 bits
  Bit[1:0]: Scaling man mode horizontal scale factor high 2 bits

  to:

  Bit[7]: Scaling mode vertical output size bit[0] (11 bits total).
  For others, refer to registers REGB8[7:6] and REGBC
  Bit[6:4]: Scaling mode horizontal output size bit[2:1] (11 bits total). For others, refer to register REGBB
  Bit[3:0]: Reserved

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 5 on page 22, changed name, default value, and R/W of register 0xB8 from “RSVD”, “XX” and “–” to “REGB8”, “00”, and “RW”, respectively
- In Table 5 on page 22, changed decription of register 0xB8 from “Reserved” to:

  Register B8

  Bit[7:6]: Scaling mode vertical output size bit[2:1] (11 bits total). For others, refer to registers REGB7[7] and REGBC

  Bit[5:3]: Scaling mode vertical input size bit[2:0] (11 bits total). For others, refer to register REGBA

  Bit[2:0]: Scaling mode horizontal input size bit[2:0] (11 bits total). For others, refer to register REGB9
- In Table 5 on page 22, changed name, default value, R/W and description of register 0xB9 from “RSVD”, “XX”, “–” and “Reserved” to “REGB9”, “A0”, “RW” and “Scaling Mode Horizontal Input Size bit[10:3] (11 bits total). For others, refer to register REGB8[2:0]”, respectively
- In Table 5 on page 22, changed name, default value, R/W and description of register 0xBA from “RSVD”, “XX”, “–” and “Reserved” to “REGBA”, “80”, “RW” and “Scaling Mode Vertical Input Size bit[10:3] (11 bits total). For others, refer to register REGB8[5:3]”, respectively
- In Table 5 on page 22, changed name, default value, R/W and description of register 0xBB from “RSVD”, “XX”, “–” and “Reserved” to “REGBB”, “A0”, “RW” and “Scaling Mode Horizontal Output Size[10:3] (11 bits total). For others, refer to registers REGB8[7:6] and REGB7[6:4]”, respectively
- In Table 5 on page 22, changed name, default value, R/W and description of register 0xBC from “RSVD”, “XX”, “–” and “Reserved” to “REGBC”, “80”, “RW” and “Scaling Mode Vertical Output Size[10:3] (11 bits total). For others refer to registers REGB7[7] and REGB8[7:6]”, respectively
- In Table 5 on page 22, changed name, default value, R/W and description of register 0xBD from “RSVD”, “XX”, “–” and “Reserved” to “CMX1”, “09”, “RW” and “Color Matrix Parameter 1”
- In Table 5 on page 22, changed name, default value, R/W and description of register 0xBE from “RSVD”, “XX”, “–” and “Reserved” to “CMX2”, “13”, “RW” and “Color Matrix Parameter 2”
- In Table 5 on page 22, changed name, default value, R/W and description of register 0xBF from “RSVD”, “XX”, “–” and “Reserved” to “CMX3”, “04”, “RW” and “Color Matrix Parameter 3”
- In Table 5 on page 22, added “Y = (CMX1 × R + CMX2 × G + CMX3 × B) / 32” to the description of registers CMX1 (0xBD), CMX2 (0xBE), and CMX3 (0xBF)
- In Table 5 on page 22, changed name, default value, R/W and description of register 0xC0 from “RSVD”, “XX”, “–” and “Reserved” to “CMX4”, “0A”, “RW” and “Color Matrix Parameter 4”
- In Table 5 on page 22, changed name, default value, R/W and description of register 0xC1 from “RSVD”, “XX”, “–” and “Reserved” to “CMX5”, “12”, “RW” and “Color Matrix Parameter 5”

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 5 on page 22, changed name, default value, R/W and description of register 0xC2 from “RSVD”, “XX”, “–” and “Reserved” to “CMX6”, “1C”, “RW” and “Color Matrix Parameter 6”
- In Table 5 on page 22, added “U = (CMX4 × R + CMX5 × G + CMX6 × B) / 32” to the description of registers CMX4 (0xC0), CMX5 (0xC1), and CMX6 (0xC2)
- In Table 5 on page 23, changed name, default value, R/W and description of register 0xC3 from “RSVD”, “XX”, “–” and “Reserved” to “CMX7”, “1C”, “RW” and “Color Matrix Parameter 7”
- In Table 5 on page 23, changed name, default value, R/W and description of register 0xC4 from “RSVD”, “XX”, “–” and “Reserved” to “CMX8”, “16”, “RW” and “Color Matrix Parameter 8”
- In Table 5 on page 23, changed name, default value, R/W and description of register 0xC5 from “RSVD”, “XX”, “–” and “Reserved” to “CMX9”, “04”, “RW” and “Color Matrix Parameter 9”
- In Table 5 on page 23, added “V = (CMX7 × R + CMX8 × G + CMX9 × B) / 32” to the description of registers CMX7 (0xC3), CMX8 (0xC4), and CMX9 (0xC5)
- In Table 5 on page 23, changed name, default value, and R/W of register 0xC6 from “RSVD”, “XX” and “–” to “CMX10”, “98”, and “RW”, respectively
- In Table 5 on page 23, changed decription of register 0xC6 from “Reserved” to:

  Color Matrix Control 1

  Bit[7]: Sign bit of CMX8
  Bit[6]: Sign bit of CMX7
  Bit[5]: Sign bit of CMX6
  Bit[4]: Sign bit of CMX5
  Bit[3]: Sign bit of CMX4
  Bit[2]: Sign bit of CMX3
  Bit[1]: Sign bit of CMX2
  Bit[0]: Sign bit of CMX1
- In Table 5 on page 23, changed nameof register 0xC7 from “ISPCOM4” to “CMX11”

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 5 on page 23, changed decription of register 0xC7 from:

  Bit[7:5]: Reserved
  Bit[4]: SDE
  Bit[3:0]: Reserved

  to:

  Color Matrix Control 2
  - Bit[7]: Sign bit of CMX9
  - Bit[6]: Reserved
  - Bit[5]: Auto UV adjustment enable
    - 0: Disable
    - 1: Enable
  - Bit[4]: Special Digital Effects (SDE) enable
    - 0: Disable
    - 1: Enable
  - Bit[3:0]: Reserved
- In Table 5 on page 24, changed name, default value, and R/W of register 0xC8 from “RSVD”, “XX” and “–” to “REGC8”, “00”, and “RW”, respectively
- In Table 5 on page 24, changed decription of register 0xC8 from “Reserved” to:

  Register C8
  - Bit[7]: Fixed Y output value
    - 0: Disable
    - 1: Enable
  - Bit[6]: Negative output
    - 0: Disable
    - 1: Enable
  - Bit[5]: Gray scale output
    - 0: Disable
    - 1: Enable
  - Bit[4]: Fixed V output value
    - 0: Disable
    - 1: Enable
  - Bit[3]: Fixed U output value
    - 0: Disable
    - 1: Enable
  - Bit[2]: Contrast function enable
    - 0: Disable
    - 1: Enable
  - Bit[1]: Color saturation function enable
    - 0: Disable
    - 1: Enable
  - Bit[0]: Hue adjustment enable
    - 0: Disable
    - 1: Enable
- In Table 5 on page 24, changed name, default value, R/W and description of register 0xC9 from “RSVD”, “XX”, “–” and “Reserved” to “REGC9”, “00”, “RW” and “Hue Adjustment Cosine Parameter”

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 5 on page 24, changed name, default value, R/W and description of register 0xCA from “RSVD”, “XX”, “–” and “Reserved” to “REGCA”, “80”, “RW” and “Hue Adjustment Sine Parameter”
- In Table 5 on page 24, changed name, default value, R/W and description of register 0xCB from “RSVD”, “XX”, “–” and “Reserved” to “REGCB”, “40”, “RW” and “Saturation U Gain Value”
- In Table 5 on page 24, changed name, default value, R/W and description of register 0xCC from “RSVD”, “XX”, “–” and “Reserved” to “REGCC”, “40”, “RW” and “Saturation V Gain Value”
- In Table 5 on page 24, changed name, default value, R/W and description of register 0xCD from “RSVD”, “XX”, “–” and “Reserved” to “REGCD”, “80”, “RW” and “Fixed U Output Value”
- In Table 5 on page 24, changed name, default value, R/W and description of register 0xCE from “RSVD”, “XX”, “–” and “Reserved” to “REGCE”, “80”, “RW” and “Fixed V Output Value”
- In Table 5 on page 24, changed name, default value, R/W and description of register 0xCF from “RSVD”, “XX”, “–” and “Reserved” to “REGCF”, “00”, “RW” and “Y Offset Value”
- In Table 5 on page 24, changed name, default value, R/W and description of register 0xD0 from “RSVD”, “XX”, “–” and “Reserved” to “REGD0”, “20”, “RW” and “Y Gain Value”
- In Table 5 on page 24, changed name, default value, R/W and description of register 0xD1 from “RSVD”, “XX”, “–” and “Reserved” to “REGD1”, “00”, “RW” and “Y Brightness Value”
- In Table 5 on page 24, added “Y’ = [(Y + Yoffset) × Ygain] + Ybrightness when enabling contrast function” to the description of registers REGCF (0xCF), REGD0 (0xD0), and REGD1 (0xD1)
- In Table 5 on page 25, changed name of register 0xD5 from “UVCOM” to “REGD5”

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 5 on page 25, changed decription of register 0xD5 from:

  Bit[7]: UV adjust
  Bit[6:0]: Reserved

  to:

  IO Pad Direction Control

  Bit[7]: D7 direction control
  0: Output
  1: Input
  Bit[6]: D6 direction control
  0: Output
  1: Input
  Bit[5]: D5 direction control
  0: Output
  1: Input
  Bit[4]: D4 direction control
  0: Output
  1: Input
  Bit[3]: D3 direction control
  0: Output
  1: Input
  Bit[2]: D2 direction control
  0: Output
  1: Input
  Bit[1]: D1 direction control
  0: Output
  1: Input
  Bit[0]: D0 direction control
  0: Output
  1: Input

- In Table 5 on page 25, changed name, default value, and R/W of register 0xD6 from “RSVD”, “XX” and “–” to “REGD6”, “00”, and “RW”, respectively
- In Table 5 on page 25, changed decription of register 0xD6 from “Reserved” to:

  Register D6

  Bit[7:2]: Reserved
  Bit[1]: D9 direction control
  0: Output
  1: Input
  Bit[0]: D8 direction control
  0: Output
  1: Input

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 5 on page 25, changed name, default value, and R/W of register 0xD7 from “RSVD”, “XX” and “–” to “REGD7”, “03”, and “RW”, respectively
- In Table 5 on page 25, changed decription of register 0xD7 from “Reserved” to:

Register D7

Bit[7:5]: Reserved
Bit[4]: YU swap function enable
0: Disable
1: Enable
Bit[3]: Data pins swap function (changes MSB to D0 and LSB to D9)
0: Disable
1: Enable
Bit[2]: Reserved
Bit[1:0]: Data output format selection
00: YUV output
01: RGB output
10: Not used
11: RAW output

- In Table 5 on page 25, changed name, default value, and R/W of register 0xD8 from “RSVD”, “XX” and “–” to “REGD8”, “C4”, and “RW”, respectively
- In Table 5 on page 25, changed decription of register 0xD8 from “Reserved” to:

Register D8

Bit[7:4]: Reserved
Bit[3]: CCIR656 output selection
0: Disable
1: Enable
Bit[2]: Reserved
Bit[1:0]: RGB data output format selection (effective when register bits REGD7[1:0] = 11
00: Not used
01: RGB565
10: RGB555
11: RGB444

REVISION CHANGE LIST

Document Title: OV9660 (CSP2) Datasheet **Version:** 1.4

DESCRIPTION OF CHANGES

The following changes were made to version 1.3:

- In the Key Specifications table on page 1, added footnote “a” to Standby Power Requirements
- In Table 3 on page 5, changed Typ spec for Standby current ($I_{DDS-SCCB}$) from “1” to “2”
- In Table 3 on page 5, added footnote “a” to Typ specification for Standy current ($I_{DDS-SCCB}$) and Max specification for Standby current ($I_{DDS-PWDN}$)
- In Figure 6 on page 8, deleted HSYNC timing
- In Figure 7 on page 8, deleted HSYNC timing and changed figure title from “VGA Frame Timing” to “VGA 60 Frame Timing”
- Deleted figures for QVGA Frame Timing, QQVGA Frame Timing, CIF Frame Timing, QCIF Frame Timing, QQCIF Frame Timing
- In Table 5 on page 13, changed description of register bits COM7[6:5] (0x12) from:

  Bit[6:5]: Resolution selection
  00: SXGA (full size) mode
  01: VGA mode
  10: Not used
  11: Not used

  to

  Bit[6:5]: Resolution selection
  00: SXGA (full size) mode
  01: Not used
  10: VGA mode
  11: Not used
- In Table 5 on page 13, changed description of register bit COM8[6] (0x13) from “Reserved” to “AEC step size limit”

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 5 on page 14, changed description of register bits COM9[7:5] (0x14) from:

  Bit[7:5]: AGC gain ceiling
  000: 2x
  001: 4x
  010: 8x
  011: 16x
  100: 32x
  101: 64x
  110: 128x
  111: 128x

  to

  Bit[7:5]: AGC gain ceiling
  000: 2x
  001: 4x
  010: 8x
  011: 16x
  100: 32x
  101: Not used
  110: Not used
  111: Not used

- In Table 5 on page 14, changed description of register bits COM9[3:1] (0x14) from "Reserved" to:

  Bit[3]: Exposure time can be less than limitation of banding filter when light is too strong
  Bit[2]: Data output format - VSYNC drop option
  0: VSYNC always exists
  1: VSYNC will drop when frame data drops
  Bit[1]: Enable drop frame when AEC step is larger than the exposure gap

- In Table 5 on page 14, changed description of register bit COM10[0] (0x15) to "Reserved"
- In Table 5 on page 22, changed "0" and "1" descriptions for register bits REGD5[7:0] (0xD5) from "0: Output" and "1: Input" to "0: Input" and "1: Output"
- In Table 5 on page 22, changed "0" and "1" descriptions for register bits REGD6[1:0] (0xD6) from "0: Output" and "1: Input" to "0: Input" and "1: Output"

REVISION CHANGE LIST

Document Title: OV9660 (CSP2) Datasheet **Version:** 1.5

DESCRIPTION OF CHANGES

The following changes were made to version 1.4:

- In the Key Specifications table on page 1, deleted specification for Core Power Supply
- In the Key Specifications table on page 1, deleted table footnote a
- In the Key Specifications table on page 1, changed specification for "VGA, CIF and down scaling Maximum Image Transfer Rate" to ""VGA and down scaling Maximum Image Transfer Rate"
- In the Key Specifications table on page 1, deleted the specification for "QVGA and any lower resolution Maximum Image Transfer Rate"
- In Figure 1 on page 1, changed name of pad 13 and pad 16 from "DVDD" to "VREFD"
- In Table 1, on page 4, changed pad name, pad type and description of pads 13 and 16 from "DVDD", "Power", and "Power for digital core" to "VREFD", "Reference", and "Digital reference - connect to ground through 0.1µF capacitor", respectively for both pads
- In Table 2 on page 5, deleted Absolute Maximum Rating for V_{DD-C} Supply Voltage
- In Table 3 on page 5, deleted specification for DC supply voltage - Core (V_{DD-C})
- In Table 3 on page 5, changed symbol for Active (operating) current from "I_{DDA-A}" to "I_{DDA}"
- In Table 3 on page 5, added "See Note [a]" to Active (operating) current specification under Condition and added table footnote a
- In Table 3 on page 5, changed Typ specification for Active (operating) current from "TBD" to "11 + 18[b]" and added table footnote b
- In Table 3 on page 5, deleted specifications for Active (operating) current for I_{DDA-D} and I_{DD-IO}
- In Table 3 on page 5, changed Typ specification for Standby current ($I_{DDS-SCCB}$) from "2[a]" to "1" and added Max specification "2"
- In Table 3 on page 5, changed Max spec for Standby current ($I_{DDS-PWDN}$) from "20[a]" to "20"
- In Table 3 on page 5, added "See Note [c]" to Standby current specifications under Condition and added table footnote c
- In Table 4 on page 6, deleted "V_{DD-D} = 1.2V" from AC Conditions at bottom of table

DESCRIPTION OF CHANGES (CONTINUED)

- In Figure 7 on page 8, changed figure title from “VGA 60 Frame Timing” to “VGA 30 Frame Timing”
- In Figure 7 on page 8, changed callouts from “4 x t_{LINE}” to “3033.5 tp”, from “18341 tp” to “18349.5 tp”, and from “13712 tp” to “13679 tp”
- In Table 5 on page 11, changed register name, default value, and R/W type of register 0x06 from “RSVD”, “XX” and “–” to “REG06”, “10” and “RW”, respectively
- In Table 5 on page 11, changed description of register 0x06 from “Reserved” to:

  Register 06
  - Bit[7:6]: Dummy line insertion trigger point
    - 00: Dummy line insertion begins from 2x gain
    - 01: Dummy line insertion begins from 4x gain
    - 10: Dummy line insertion begins from 8x gain
    - 11: Reserved
  - Bit[5:0]: Reserved
- In Table 5 on page 16, changed register name, default value, R/W type and description of register 0x3B to “RSVD”, “XX”, “–” and “Reserved”, respectively
- In Table 5 on page 16, changed register name, default value, and R/W type of register 0x3E from “RSVD”, “XX” and “–” to “REG3E”, “50” and “RW”, respectively
- In Table 5 on page 16, changed description of register 0x3E from “Reserved” to:

  Register 3E
  - Bit[7]: PLL bypass option
    - 0: Enable PLL
    - 1: Bypass PLL
  - Bit[6:0]: Reserved
- In Table 5 on page 16, changed register name, default value, and R/W type of register 0x43 from “RSVD”, “XX” and “–” to “REG43”, “00” and “RW”, respectively
- In Table 5 on page 16, changed description of register 0x43 from “Reserved” to:

  Register 43
  - Bit[7]: 9-Zone average option
    - 0: Full size and VGA30
    - 1: Other size
  - Bit[6:0]: Reserved
- In Table 5 on page 17, changed register name, default value, and R/W type of register 0x5C from “RSVD”, “XX” and “–” to “REG5C”, “00” and “RW”, respectively

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 5 on page 17, changed description of register 0x5C from “Reserved” to:

  Register 5C
  - Bit[7]: Average AEC option
    - 0: 9-zone average AEC
    - 1: Full average AEC
  - Bit[6:0]: Reserved

- In Table 5 on page 18, changed register name, default value, and R/W type of register 0x64 from “RSVD”, “XX” and “–” to “REG64”, “24” and “RW”, respectively
- In Table 5 on page 18, changed description of register 0x64 from “Reserved” to:

  Register 5C
  - Bit[7]: BLC line select
    - 0: SXGA
    - 1: Other resolution
  - Bit[6:0]: Reserved

- In Table 5 on page 19, changed desription of register bit REGAB[3] (0xAB) from “Scaling man enable option” to “Scaling enable option”
- In Table 5 on page 19, changed desription of register bit REGAB[2] (0xAB) from “Scaling enable option” to “Sharpness enable option”
- In Table 5 on page 23, changed description of register bit REGD7[2] (0xD7) from “Reserved” to:

  Bit[2]: HREF to HSYNC
  - 0: Output HREF signal
  - 1: Output HSYNC signal

- In Table 5 on page 23, changed description of register bits REGD7[1:0] (0xD7) to:

  Bit[1:0]: Data output format selection
  - 00: YUV output
  - 01: RGB output
  - 10: ISP RAW output
  - 11: Sensor RAW output

- In Table 5 on page 23, changed description of register bit REGD8[5] (0xD8) from “Reserved” to:

  Bit[5]: HREF negative
  - 0: Positive
  - 1: Negative

- In Figure 13 on page 26, replaced IR Reflow Profile graph

REVISION CHANGE LIST

Document Title: OV9660 (CSP2) Datasheet **Version:** 1.6

DESCRIPTION OF CHANGES

The following changes were made to version 1.5:

- Under General Description on page 1, changed “white pixel canceling” to “defect pixel canceling” in the second paragraph
- Under Features on page 1, changed “white pixel canceling” to “defect pixel canceling” in the seventh bullet item
- In the Key Specifications table on page 1, changed Active Power Requirements from “120 mW typical (15fps, no I/O power)” to “80 mW typical (15fps)”
- In the Key Specifications table on page 1, changed Standby Power Requirements from “< 20 µA” to “15 µA typical”
- In the Key Specifications table on page 1, changed Temperature Range specification from “-20°C to 70°C” to “-30°C to 70°C”
- In the Key Specifications table on page 1, changed Lens Size from 1/5" to 1/5.5"
- In the Key Specifications table on page 1, changed Chief Ray Angle from “TBD” to “25° non-linear”
- In the Key Specifications table on page 1, changed Sensitivity from “TBD” to “450 mV/(Lux • sec)”
- In the Key Specifications table on page 1, changed S/N Ratio from “TBD” to “40 dB”
- In the Key Specifications table on page 1, changed Dynamic Range from “TBD” to “55 dB”
- In the Key Specifications table on page 1, changed Dark Current from “TBD” to “3 mV/sec @ 60°C”
- In the Key Specifications table on page 1, changed Well Capacity from “TBD” to “13 Ke”
- In the Key Specifications table on page 1, changed Fixed Pattern Noise from “TBD” to “1% of $V_{PEAK-TO-PEAK}$”
- In Figure 2 on page 2, changed note 1 from “... de-noise, white/black pixel correction, ...” to “... de-noise, defect pixel correction, ...”
- Under A/D Converters on page 3, changed the second sentence from “... speeds up to 13 MHz ...” to “... speeds up to 27 MHz ...”
- Under Digital Signal Procesor (DSP) on page 3, changed the eighth bullet item from “White pixel canceling” to “Defect pixel canceling”
- In Table 1 on page 4, changed description of pin A1 from “... connect to ground ...” to “... connect to analog ground ...”

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 1 on page 4, changed description of pin A2 from "... connect to ground ..." to "... connect to analog ground ..."
- In Table 1 on page 4, changed description of pin E4 from "... connect to ground through 0.1 µF capacitor" to "... connect to digital ground through a 0.1 µF capacitor and connect with pin F3"
- In Table 1 on page 4, changed description of pin F1 from "... digital video port" to "... digital / video port"
- In Table 1 on page 4, changed description of pin F2 from "... digital video port" to "... digital / video port"
- In Table 1 on page 4, changed description of pin F3 from "... connect to ground through 0.1 µF capacitor" to "... connect to digital ground through a 0.1 µF capacitor and connect with pin E4"
- In Table 2 on page 5, changed Absolute Maximum Rating for V_{DD-IO} Supply Voltage from "3 V" to "4.5 V"
- In Table 3 on page 5, changed Typ for Active (operating) current from "11 + 18[b]" to "17 + 18[b]" and added "50" for Max
- In Table 3 on page 5, added "2" for Max Standby current ($I_{DDS-SCCB}$)
- In Table 3 on page 5, added "15" for Typ Standby current ($I_{DDS-PWDN}$) and "30" for Max Standby current ($I_{DDS-PWDN}$)
- In Table 3 on page 5, changed table footnote a from "..., f_{CLK} = 24MHz at 7.5 fps YCbCr output, no I/O loading" to "..., f_{CLK} = 24MHz at 15 fps YCbCr output with typical loading"
- In Table 3 on page 5, changed table footnote b from "I_{DD-IO} = 11mA, I_{DD-A} = 18mA, without loading" to "I_{DD-IO} = 17mA, I_{DD-A} = 18mA, with typical loading"
- In Table 4 on page 6, added "with PLL" to Input clock frequency (f_{CLK}) specification and added Min of "10" and Max of "27"
- In Table 4 on page 6, added a row for Input clock frequency (f_{CLK}) "without PLL" with a Min, Typ and Max of "10", "24" and "54", respectively
- In Table 4 on page 6, changed AC Conditions for V_{DD} from "V_{DD-IO} = 2.8V" to "V_{DD-IO} = 1.8V" and for Output Loading from "25pF, 1.2KΩ to 2.8V" to "20pF"
- Under Timing Specifications on page 7, added note "Timing may vary depending on register settings"
- Under Register Set on page 11, added note "Reserved registers or register bits may be non-functional, special function or sensitive to the sensor. Please refer to OmniVision's recommended register settings."
- In Table 5 on page 11, changed default value of register COM1 (0x03) from "0F" to "03"

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 5 on page 11, changed description of register bits REG04[4:3] (0x04) to “Reserved”
- In Table 5 on page 11, changed name, default value, and R/W type for register 0x05 from “RSVD”, “XX” and “–” to “REG05”, “00” and “RW”, respectively
- In Table 5 on page 11, changed description of register 0x05 from “Reserved” to:

  Register 05

  Bit[7:3]: Reserved

  Bit[2:0]: UV adjust slope[5:3] between gain threshold 1 and gain threshold 2. For others, refer to registers COM1[5:4] (0x03) and REG60[2:0] (0x60).
- In Table 5 on page 12, changed description of register bits REG06[7:6] (0x06) from:

  Bit[7:6]: Dummy line insertion trigger point

  00: Dummy line insertion begins from 2x gain

  01: Dummy line insertion begins from 4x gain

  10: Dummy line insertion begins from 8x gain

  11: Reserved

  to:

  Bit[7:6]: Dummy line insertion beginning gain

  00: 2x

  01: 4x

  10: 8x

  11: 8x
- In Table 5 on page 12, added “(SCCB standby mode)” to description of register bit COM2[4] (0x09)
- In Table 5 on page 12, changed default value for register VER (0x0B) from “60” to “63”
- In Table 5 on page 13, changed default value of register COM6 (0x0F) from “42” to “46”
- In Table 5 on page 13, changed default value of register AEC (0x10) from “41” to “00”
- In Table 5 on page 13, changed default value of register CLKRC (0x11) from “00” to “80”
- In Table 5 on page 13, changed description of register bit CLKRC[6] (0x11) to “Reserved” and added “for frame rate adjustment” to description of register bits CLKRC[5:0] (0x11)
- In Table 5 on page 13, changed description of register bit COM7[3] (0x12) to “Reserved”
- In Table 5 on page 13, added “or 1/100s” to description of ‘1’ for register bit COM8[5] (0x13)
- In Table 5 on page 14, added “(1/120” or 1/100s)” to description of register bit COM9[3] (0x14)
- In Table 5 on page 14, added “(works on row data output)” to description of register bit COM10[5] (0x15) and changed description of register bits COM10[4:3] (0x15) to “Reserved”
- In Table 5 on page 15, changed default value of register REG1E (0x1E) from “C8” to “F9”
- In Table 5 on page 15, changed description for register REG2B (0x2B) from “... in SXGA and 1/769 Tframe ...” to “... in SXGA and 1/760 Tframe ...”
- In Table 5 on page 17, changed default value of register REG33 (0x33) from “00” to “C0”

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 5 on page 17, changed name, default value, and R/W type for register 0x36 from “RSVD”, “XX” and “–” to “REG36”, “94” and “RW”, respectively
- In Table 5 on page 17, changed description of register 0x36 from “Reserved” to:

  Register 36

  Bit[7:6]: Reserved
  Bit[5]: Auto de-noise divider value
  0: 128
  1: 64
  Bit[4:0]: Reserved
- In Table 5 on page 17, changed name, default value, and R/W type for register 0x3B from “RSVD”, “XX” and “–” to “REG3B”, “00” and “RW”, respectively
- In Table 5 on page 17, changed description of register 0x3B from “Reserved” to:

  Power Control 3B

  Bit[7:4]: Reserved
  Bit[3]: Bypass internal regulator
  0: Use internal regulator to generate V_{DD-D} power
  1: Bypass internal regulator (V_{DD-D} power needs to be provided by an external source)
  Bit[2:0]: Reserved
- In Table 5 on page 17, changed name, default value, and R/W type for register 0x3D from “RSVD”, “XX” and “–” to “REG3D”, “3C” and “RW”, respectively
- In Table 5 on page 17, changed description of register 0x3D from “Reserved” to:

  Common Control 3D

  Bit[7:6]: Reserved
  Bit[5:0]: PLL divider
  f_{CLK} = XCLK × (0x40 – REG3D[5:0]) / 8 / (CLKRC[5:0] + 1)
- In Table 5 on page 17, changed name, default value, and R/W type for register 0x41 from “RSVD”, “XX” and “–” to “REG41”, “00” and “RW”, respectively
- In Table 5 on page 17, changed description of register 0x41 from “Reserved” to:

  Register 41

  Bit[7:5]: UV adjust offset value[5:3] between gain threshold 1 and gain threshold 2. For others, refer to register REG5B[4:2] (0x5B).
  Bit[4:0]: Reserved
- In Table 5 on page 17, changed description of register bit REG43[7] (0x43) from “9-Zone average option” to “9-zone average AEC option”
- In Table 5 on page 17, changed default value of register COM22 (0x4B) from “20” to “00”
- In Table 5 on page 18, changed name, default value, and R/W type for register 0x5A from “RSVD”, “XX” and “–” to “REG5A”, “57” and “RW”, respectively
- In Table 5 on page 18, changed description of register 0x5A from “Reserved” to:

  Register 5A

  Bit[7:4]: 50 Hz banding maximum AEC step
  Bit[3:0]: 60 Hz banding maximum AEC step
- In Table 5 on page 18, changed name, default value, and R/W type for register 0x5B from “RSVD”, “XX” and “–” to “REG5B”, “20” and “RW”, respectively

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 5 on page 18, changed description of register 0x5B from “Reserved” to:

  Register 5B

  Bit[7:5]: Reserved

  Bit[4:2]: UV adjust offset value[5:3] between gain threshold 1 and gain threshold 2. For others, refer to register REG41[7:5] (0x41).

  Bit[1:0]: Reserved
- In Table 5 on page 18, changed name, default value, and R/W type for register 0x60 from “RSVD”, “XX” and “–” to “REG60”, “80” and “RW”, respectively
- In Table 5 on page 18, changed description of register 0x60 from “Reserved” to:

  Register 60

  Bit[7:3]: Reserved

  Bit[2:0]: UV adjust slope[2:0] between gain threshold 1 and gain threshold 2. For others, refer to registers COM1[5:4] (0x03) and REG05[2:0] (0x05).
- In Table 5 on page 18, changed default value of register REG64 (0x64) from “24” to “20”
- In Table 5 on page 18, changed description of register REG64 (0x64) from:

  Register 64

  Bit[7]: BLC line select

  1: Other resolution

  0: SXGA

  Bit[6:0]: Reserved

  to:

  Register 64

  Bit[7]: BLC line select

  0: SXGA

  1: Other resolution

  Bit[6:0]: Reserved
- In Table 5 on page 19, changed name, default value, and R/W type for register 0x65 from “RSVD”, “XX” and “–” to “REG65”, “10” and “RW”, respectively
- In Table 5 on page 19, changed description of register 0x65 from “Reserved” to:

  Register 65

  Bit[7:2]: Reserved

  Bit[1:0]: UV adjustment gain threshold 2 value[4:3]
- In Table 5 on page 19, changed name, default value, and R/W type for register 0x66 from “RSVD”, “XX” and “–” to “REG66”, “00” and “RW”, respectively
- In Table 5 on page 19, changed description of register 0x66 from “Reserved” to:

  Register 66

  Bit[7:5]: UV adjustment gain threshold 2 value[2:0]

  Bit[4:0]: Reserved
- In Table 5 on page 19, changed name, default value, and R/W type for register 0x6A from “RSVD”, “XX” and “–” to “REG6A”, “24” and “RW”, respectively

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 5 on page 19, changed description of register 0x6A from “Reserved” to:

  Register 6A

  Bit[7:5]: Reserved
  Bit[4]: FIFO manual option (works with scaling function)
  0: Auto mode
  1: Manual mode
  Bit[3:0]: Reserved
- In Table 5 on page 19, changed name, default value, and R/W type for register 0x75 from “RSVD”, “XX” and “–” to “REG75”, “D0” and “RW”, respectively
- In Table 5 on page 19, changed description of register 0x75 from “Reserved” to:

  Histogram-based AEC Lower Limit of Probability - LPH
- In Table 5 on page 19, changed name, default value, and R/W type for register 0x76 from “RSVD”, “XX” and “–” to “REG76”, “D0” and “RW”, respectively
- In Table 5 on page 19, changed description of register 0x76 from “Reserved” to:

  Histogram-based AEC Upper Limit of Probability - UPL
- In Table 5 on page 19, changed name, default value, and R/W type for register 0x77 from “RSVD”, “XX” and “–” to “REG77”, “F0” and “RW”, respectively
- In Table 5 on page 19, changed description of register 0x77 from “Reserved” to:

  Histogram-based AEC Probability Threshold for LRL - TPL
- In Table 5 on page 19, changed name, default value, and R/W type for register 0x78 from “RSVD”, “XX” and “–” to “REG78”, “90” and “RW”, respectively
- In Table 5 on page 19, changed description of register 0x78 from “Reserved” to:

  Histogram-based AEC Probability Threshold for HRL - TPH
- In Table 5 on page 19, changed name, default value, and R/W type for register 0x79 from “RSVD”, “XX” and “–” to “REG79”, “E5” and “RW”, respectively
- In Table 5 on page 19, changed description of register 0x79 from “Reserved” to:

  Register 79

  Bit[7:2]: High nibble of luminance thrreshold for AEC/AGC speed control
  Bit[3:0]: Low nibble of luminance threshold for AEC/AGC speed control
- In Table 5 on page 19, changed name, default value, and R/W type for register 0x7D from “RSVD”, “XX” and “–” to “REG7D”, “00” and “RW”, respectively
- In Table 5 on page 19, changed description of register 0x7D from “Reserved” to:

  Lens Correction Center Coordinates X

  Bit[7]: Sign bit
  Bit[6:0]: X-coordinate for lens correction center
- In Table 5 on page 19, changed name, default value, and R/W type for register 0x7E from “RSVD”, “XX” and “–” to “REG7E”, “00” and “RW”, respectively
- In Table 5 on page 19, changed description of register 0x7E from “Reserved” to:

  Lens Correction Center Coordinates Y

  Bit[7]: Sign bit
  Bit[6:0]: Y-coordinate for lens correction center

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 5 on page 19, changed name, default value, and R/W type for register 0x7F from “RSVD”, “XX” and “–” to “REG7F”, “18” and “RW”, respectively
- In Table 5 on page 19, changed description of register 0x7F from “Reserved” to:

  Radius of the Circular Section Where Lens Correction Is Not Needed
- In Table 5 on page 19, changed name, default value, and R/W type for register 0x80 from “RSVD”, “XX” and “–” to “REG80”, “04” and “RW”, respectively
- In Table 5 on page 19, changed description of register 0x80 from “Reserved” to:

  Lens Correction Blue Gain Parameter - this register is valid when register LC7[2] (0x83) = 1
- In Table 5 on page 19, changed name, default value, and R/W type for register 0x81 from “RSVD”, “XX” and “–” to “REG81”, “04” and “RW”, respectively
- In Table 5 on page 19, changed description of register 0x81 from “Reserved” to:

  Lens Correction Red Gain Parameter - this register is valid when register LC7[2] (0x83) = 1
- In Table 5 on page 20, changed name, default value, and R/W type for register 0x82 from “RSVD”, “XX” and “–” to “REG82”, “04” and “RW”, respectively
- In Table 5 on page 20, changed description of register 0x82 from “Reserved” to:

  Lens correction Green Gain Parameter
- In Table 5 on page 20, changed description of register bit LC7[2] (0x83) from “Reserved” to:

  Bit[2]: Lens correction control select
  - 0: Use register REG82 (0x82) for gain parameter for R, G, and B channels
  - 1: Use register REG82 (0x82) for green gain parameter, register REG80 (0x80) for blue gain parameter, and register REG81 (0x81) for red gain parameter
- In Table 5 on page 20, changed name, default value, and R/W type for register 0x84 from “RSVD”, “XX” and “–” to “REG84”, “86” and “RW”, respectively
- In Table 5 on page 20, changed description of register 0x84 from “Reserved” to:

  De-noise Level
- In Table 5 on page 20, changed description of register bits REG85[4:3] (0x85) from:

  Bit[4]: RAW/YUV
  Bit[3]: Reserved

  to:

  Bit[4]: RAW/YUV (only works when register bits REGD7[1:0] (0xD7) = 0’b10)
  Bit[3]: FIFO enable (works with scaling function)
- In Table 5 on page 20, changed default value for register GAM1 (0x9B) from “0E” to “04”
- In Table 5 on page 20, changed default value for register GAM2 (0x9C) from “1A” to “07”
- In Table 5 on page 20, changed default value for register GAM3 (0x9D) from “31” to “10”
- In Table 5 on page 20, changed default value for register GAM4 (0x9E) from “5A” to “28”
- In Table 5 on page 20, changed default value for register GAM5 (0x9F) from “69” to “36”
- In Table 5 on page 20, changed default value for register GAM6 (0xA0) from “75” to “44”

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 5 on page 20, changed default value for register GAM7 (0xA1) from “7E” to “52”
- In Table 5 on page 20, changed default value for register GAM8 (0xA2) from “88” to “60”
- In Table 5 on page 20, changed default value for register GAM9 (0xA3) from “8F” to “6C”
- In Table 5 on page 20, changed default value for register GAM10 (0xA4) from “96” to “78”
- In Table 5 on page 21, changed default value for register GAM11 (0xA5) from “A3” to “8C”
- In Table 5 on page 21, changed default value for register GAM12 (0xA6) from “AF” to “9E”
- In Table 5 on page 21, changed default value for register GAM13 (0xA7) from “C4” to “BB”
- In Table 5 on page 21, changed default value for register GAM14 (0xA8) from “D7” to “D2”
- In Table 5 on page 21, changed default value for register GAM15 (0xA9) from “E8” to “E5”
- In Table 5 on page 21, changed default value for register SLOP (0xAA) from “20” to “24”
- In Table 5 on page 21, changed name, default value, and R/W type for register 0xAC from “RSVD”, “XX” and “–” to “REGAC”, “02” and “RW”, respectively
- In Table 5 on page 21, changed description of register 0xAC from “Reserved” to:

  De-noise Offset Limit in Auto De-noise Mode
- In Table 5 on page 21, changed name, default value, and R/W type for register 0xAD from “RSVD”, “XX” and “–” to “REGAD”, “25” and “RW”, respectively
- In Table 5 on page 21, changed description of register 0xAD from “Reserved” to:

  Register AD

  Bit[7:5]: Reserved

  Bit[4:0]: Sharpness value when GAIN < 2x
- In Table 5 on page 21, changed name, default value, and R/W type for register 0xAE from “RSVD”, “XX” and “–” to “REGAE”, “20” and “RW”, respectively
- In Table 5 on page 21, changed description of register 0xAE from “Reserved” to:

  Register AE

  Bit[7:3]: Reserved

  Bit[2]: Sharpness threshold double

  Bit[1:0]: Reserved
- In Table 5 on page 21, changed name, default value, and R/W type for register 0xB0 from “RSVD”, “XX” and “–” to “REGB0”, “43” and “RW”, respectively

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 5 on page 21, changed description of register 0xB0 from “Reserved” to:

  Register B0

  Bit[7]: Manual de-noise mode enable
  0: Auto de-noise mode
  1: Manual de-noise

  Bit[6:0]: Reserved
- In Table 5 on page 22, changed default value for register CMX1 (0xBD) from “09” to “05”
- In Table 5 on page 22, changed default value for register CMX2 (0xBE) from “13” to “16”
- In Table 5 on page 22, changed default value for register CMX3 (0xBF) from “04” to “05”
- In Table 5 on page 22, changed default value for register CMX4 (0xC0) from “0A” to “07”
- In Table 5 on page 22, changed default value for register CMX5 (0xC1) from “12” to “18”
- In Table 5 on page 22, changed default value for register CMX6 (0xC2) from “1C” to “1F”
- In Table 5 on page 22, changed default value for register CMX7 (0xC3) from “1C” to “2B”
- In Table 5 on page 22, changed default value for register CMX8 (0xC4) from “16” to “2B”
- In Table 5 on page 22, changed default value for register CMX9 (0xC5) from “04” to “00”
- In Table 5 on page 23, changed default value for register CMX11 (0xC7) from “86” to “10”
- In Table 5 on page 23, changed default value for register REGC8 (0xC8) from “00” to “02”
- In Table 5 on page 23, changed default value for register REGC9 (0xC9) from “00” to “80”
- In Table 5 on page 23, changed default value for register REGCA (0xCA) from “80” to “00”
- In Table 5 on page 24, changed name, default value, and R/W type for register 0xD2 from “RSVD”, “XX” and “–” to “REGD2”, “00” and “RW”, respectively
- In Table 5 on page 24, changed description of register 0xD2 from “Reserved” to:

  Register D2

  Bit[7]: Auto UV adjustment enable
  Bit[6:5]: Reserved
  Bit[4:0]: UV adjust offset value after gain threshold 2
- In Table 5 on page 25, changed name, default value, and R/W type for register 0xD3 from “RSVD”, “XX” and “–” to “REGD3”, “00” and “RW”, respectively
- In Table 5 on page 25, changed description of register 0xD3 from “Reserved” to “FIFO Delay Timing Configuration (works with scaling function)”

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 5 on page 25, changed default value for register REGD7 (0xD7) from “03” to “10”
- In Table 5 on page 25, changed description of register bit REGD7[4] (0xD7) from:

  Bit[4]: YU swap function
  0: Disable
  1: Enable

  to:

  Bit[4]: YU swap function
  0: U Y V Y
  1: Y U Y V
- In Table 5 on page 25, added “- works in YUV mode” to description of register bit REGD7[3] (0xD7)
- In Table 5 on page 25, changed description of register bits REGD7[1:0] (0xD7) from:

  Bit[1:0]: Data output format selection
  00: YUV output
  01: RGB output
  10: ISP RAW output
  11: Sensor RAW output

  to:

  Bit[1:0]: Data output format selection
  00: YUV output
  01: RGB output
  10: ISP RAW output
  11: RAW output
- In Table 5 on page 25, changed description of register bit REGD8[5] (0xD8) from:

  Bit[5]: HREF negative
  0: Positive
  1: Negative

  to:

  Bit[5]: HREF/HSYNC negative output
  0: Positive output
  1: Negative output
- In Table 5 on page 25, changed description of register bits REGD8[1:0] (0xD8) from:

  Bit[1:0]: RGB data output format selection (effective when register bits REGD7[1:0] = 11
  00: Not used
  01: RGB565
  10: RGB555
  11: RGB444

  to:

  Bit[1:0]: RGB data output format selection (effective when register bits REGD7[1:0] = 01)
  00: Not used
  01: RGB565
  10: RGB555
  11: RGB444
- In Table 5 on page 25, changed name, default value, and R/W type for register 0xD9 from “RSVD”, “XX” and “–” to “REGD9”, “64” and “RW”, respectively

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 5 on page 25, changed description of register 0xD9 from “Reserved” to:

  Register D9

  Bit[7:4]: Sharpness value when 4x < GAIN < 8x

  Bit[3:0]: Sharpness value when 2x < GAIN < 4x
- In Table 5 on page 25, changed name, default value, and R/W type for register 0xDA from “RSVD”, “XX” and “–” to “REGDA”, “86” and “RW”, respectively
- In Table 5 on page 25, changed description of register 0xDA from “Reserved” to:

  Register DA

  Bit[7:4]: Sharpness value when 16x < GAIN

  Bit[3:0]: Sharpness value when 8x < GAIN < 16x
- On page 29, added subsection for Chief Ray Angle and Figure 13, OV9660 Chief Ray Angle graph